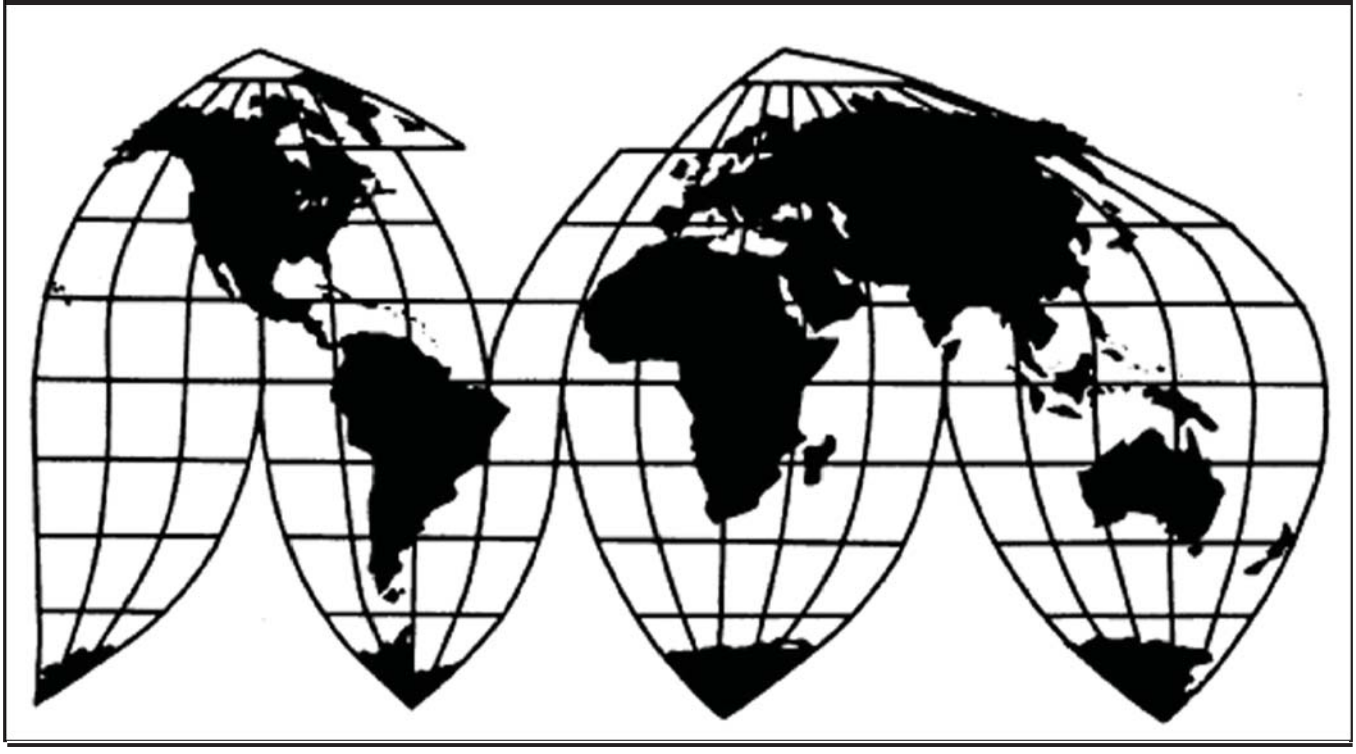
In the Matter of

Certain Integrated Circuits, Chipsets, and Products Containing Same Including Televisions

Investigation No. 337-TA-786

Publication 4406 **July 2013**

U.S. International Trade Commission



Washington, DC 20436

U.S. International Trade Commission

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UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS**	**Investigation No. 337-TA-786**

[CORRECTED] NOTICE OF COMMISSION DECISION TO REVIEW IN PART A FINAL INITIAL DETERMINATION FINDING NO VIOLATION OF SECTION 337; TERMINATION OF INVESTIGATION

AGENCY: U.S. International Trade Commission.

ACTION: Notice.

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined to review in part the presiding administrative law judge's ("ALJ") final initial determination ("ID") issued on July 12, 2012, finding no violation of section 337 of the Tariff Act of 1930, 19 U.S.C. § 1337 in the above-captioned investigation. On review, the Commission affirms the ID's finding of no violation, and terminates the investigation.

FOR FURTHER INFORMATION CONTACT: Megan M. Valentine, Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 708-2301. Copies of non-confidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-2000. General information concerning the Commission may also be obtained by accessing its Internet server at *http://www.usitc.gov*. The public record for this investigation may be viewed on the Commission's electronic docket (EDIS) at *http://edis.usitc.gov*. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on (202) 205-1810.

SUPPLEMENTARY INFORMATION: The Commission instituted this investigation on July 14, 2011, based on a complaint filed by Freescale Semiconductor, Inc. of Austin, Texas ("Freescale"). 76 *Fed. Reg.* 41521-2 (July 14, 2011). The complaint alleges violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, by reason of infringement of certain claims of U.S. Patent No. 5,467,455 ("the '455 patent"). The complaint further alleges the existence of a domestic industry. The Commission's notice of investigation named Funai Electric Co., Ltd. of Osaka, Japan and Funai Corporation, Inc. of Rutherford, New Jersey (collectively "Funai"); MediaTek Inc. of Hsinchu City, Taiwan ("MediaTek"); and Zoran

Corporation of Sunnyvale, California ("Zoran") as respondents. The Office of Unfair Import Investigations was named as a party. On May 25, 2012, the Commission determined not to review an ID (Order No. 27) terminating the investigation as to Funai on the basis of a consent order. Notice (May 25, 2012). On May 29, 2012, the Commission determined not to review an ID (Order No. 31) terminating the investigation as to certain Zoran products and certain MediaTek products. Notice (May 29, 2012).

On July 12, 2012, the ALJ issued his final ID, finding no violation of section 337 as to the '455 patent. The ID included the ALJ's recommended determination ("RD") on remedy and bonding. In particular, the ALJ found that claims 9 and 10 of the '455 patent are not invalid pursuant to 35 U.S.C. § 102, but that they are invalid pursuant to 35 U.S.C. § 103. The ALJ further found that those Zoran products that were adjudicated in *Integrated Circuits I* are precluded under the doctrine of issue preclusion. The ALJ also found that certain of the accused Zoran products remaining in the investigation infringe claims 9 and 10 of the '455 patent, but that the accused MediaTek products do not infringe claims 9 and 10 of the '455 patent. The ALJ further found that Freescale has failed to satisfy the domestic industry requirement with respect to the '455 patent. The ALJ's RD recommended a limited exclusion order barring entry of Zoran's and MediaTek's infringing integrated circuits, chipsets, and products containing same including televisions. Freescale did not request, and the ALJ did not recommend, issuance of a cease and desist order against Zoran. The ALJ also recommended that respondents be required to post no bond for the importation of products found to infringe during the period of Presidential review.

On July 24, 2012, Freescale filed a petition for review of certain aspects of the final ID's findings concerning infringement, validity, and domestic industry, and preclusion. Also on July 25, 2012, the IA timely filed a petition for review of certain aspect of the final ID's findings concerning claim construction. Further on July 24, 2012, Zoran and MediaTek contingently petitioned for review of certain aspects of the final ID's findings concerning claim construction, infringement, domestic industry, and preclusion. No post-RD statements on the public interest pursuant to Commission Rule 201.50(a)(4) or in response to the post-RD Commission Notice issued on July 16, 2012, were filed. *See* 77 *Fed. Reg.* 42764 (July 20, 2012).

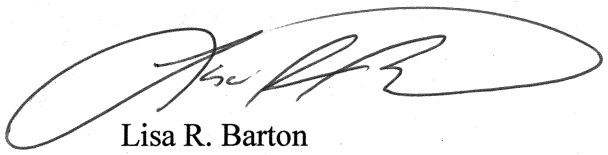
Having examined the record of this investigation, including the ALJ's final ID, the petitions for review, and the responses thereto, the Commission has determined to review the final ID in part. Specifically, the Commission has determined to review, and on review, reverses the ALJ's finding that Japanese Patent Application JP H05-83113-A to Kuboki ("Kuboki") discloses the limitation "[a] data processor within an integrated circuit package comprising: . . . a plurality of bus termination circuits" of claim 9 of the '455 patent. The Commission has also determined to review, and on review, affirms with modification the ID's finding that Kuboki in combination with the knowledge of one of ordinary skill in the art renders obvious claims 9 and 10 of the '455 patent. The Commission has further determined to review the ID's finding that the Kuboki reference in combination with U.S. Patent No. 5,479,123 to Gist ("Gist") renders obvious claims 9 and 10, and on review, finds that the Kuboki reference in combination with Gist and the knowledge of one of ordinary skill in the art renders obvious claims 9 and 10 of the '455 patent. The Commission has also determined to review the ID's finding that Freescale

failed to establish the existence of a domestic industry based on its licensing activities, and on review, affirms the ID's finding with modification. The Commission has further determined to review the ID's finding that Freescale has failed to show that the Accused Zoran Hybrid Termination Circuits infringe claims 9 and 10 of the '455 patent and on review, affirms the ID's finding with modification.

The Commission has determined not to review the remaining issues decided in the ID. A Commission opinion will issue shortly.

The authority for the Commission's determination is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in sections 210.42-46 and 210.50 of the Commission's Rules of Practice and Procedure (19 C.F.R. § 210.42-46 and 210.50).

By order of the Commission.



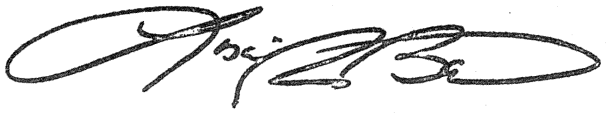
Lisa R. Barton
Acting Secretary to the Commission

Issued: September 13, 2012

CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS **337-TA-786**

CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **NOTICE** has been served by hand upon Commission Investigative Attorney **Juan S. Cockburn** and the following parties as indicated, on **September 13, 2012**



Lisa R. Barton, Acting Secretary
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CORRECTED PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS	**Investigation No. 337-TA-786**

COMMISSION OPINION

I. BACKGROUND

A. Procedural History

The Commission instituted this investigation on July 14, 2011, based on a complaint filed by Freescale Semiconductor, Inc. of Austin, Texas ("Freescale"). 76 *Fed. Reg.* 41521-2 (July 14, 2011). The complaint alleges violations of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337 ("section 337"), in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain integrated circuits, chipsets, and products containing same including televisions by reason of infringement of certain claims of U.S. Patent No. 5,467,455 ("the '455 patent"). The complaint further alleges the existence of a domestic industry. The Commission's notice of investigation named Funai Electric Co., Ltd. of Osaka, Japan and Funai Corporation, Inc. of Rutherford, New Jersey (collectively "Funai"); MediaTek Inc. of Hsinchu City, Taiwan ("MediaTek"); and Zoran Corporation of Sunnyvale, California ("Zoran") as respondents.[1] The Office of Unfair Import Investigations was named as

[1] Zoran and MediaTek supply integrated circuits, which Freescale accuses of infringing the '455

a party. The Commission later terminated Funai from the investigation on the basis of a consent order. Notice (May 25, 2012).

On July 12, 2012, the presiding administrative law judge ("ALJ") issued his final initial determination ("ID"), finding no violation of section 337 as to the '455 patent. The ID included the ALJ's recommended determination ("RD") on remedy and bonding. On July 24, 2012, Freescale filed a petition for review of certain aspects of the final ID. In particular, as relevant to this opinion, Freescale requested review of the ID's findings that the asserted claims of the '455 patent are obvious, that certain of Zoran's accused products do not infringe that patent, and that Freescale failed to satisfy the domestic industry requirement based on its investments in licensing the '455 patent. Also on July 24, 2012, respondents Zoran and MediaTek each filed contingent petitions for review of certain aspects of the ID. Further on July 25, 2012, the Commission investigative attorney ("IA") timely filed a petition for review of certain aspects of the ID. On August 1, 2012, the parties filed responses to the various petitions. No post-RD statements on the public interest pursuant to Commission Rule 201.50(a)(4) or in response to the post-RD Commission Notice (issued on July 16, 2012) were filed. *See* 77 *Fed. Reg.* 42764 (July 20, 2012).

On September 12, 2012, the Commission determined to review the final ID in part, and on review, to affirm the ID's finding of no violation of section 337 and to terminate the investigation. *See* Notice of Commission Decision to Review In Part A Final Initial Determination Finding No Violation of Section 337; Termination of Investigation (Sept. 12,

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patent, to Funai for use in the accused Funai downstream products, *e.g.*, televisions, etc. *See* Complaint at ¶¶50-89.

2012) ("Notice of Review In Part"). As discussed below, the Commission reverses the ALJ's finding that Japanese Patent Application JP H05-83113-A to Kuboki ("Kuboki") discloses the limitation "[a] data processor within an integrated circuit package comprising: . . . a plurality of bus termination circuits" of claim 9 of the '455 patent. The Commission also affirms with modification the ID's finding that Kuboki in combination with the knowledge of one of ordinary skill in the art renders obvious claims 9 and 10 of the '455 patent. The Commission further finds that the Kuboki reference in combination with U.S. Patent No. 5,479,123 to Gist ("Gist") and the knowledge of one of ordinary skill in the art renders obvious claims 9 and 10 of the '455 patent. The Commission also affirms with modification the ID's finding that Freescale has failed to show that the Accused Zoran Hybrid Termination Circuits infringe claims 9 and 10 of the '455 patent. The Commission further affirms with modification the ID's finding that Freescale failed to establish the existence of a domestic industry based on its licensing activities.

B. Patent at Issue

The '455 patent is entitled "Data Processing System and Method for Performing Dynamic Bus Termination," and is directed to a data processor that allows for dynamic termination of conductive bus lines to avoid signal reflection. Signal reflection, or transmission line effect, is a problem that occurs in devices operating at high speeds and/or high clock frequencies, as well as devices that require extremely long conductive interconnections. Signal reflection adversely affects the performance of such devices by increasing the time it takes for a voltage signal to change on the conductor or bus. In general, the claimed invention of the '455 patent allows for dynamic termination at the receiver end of a bi-directional bus to prevent signal reflection in high speed devices. A control signal in the claimed apparatus indicates whether the

device is currently receiving or sending. If the device is sending, the bus termination is enabled to dampen the incoming signal so that no reflections are sent back down the bus (transmission line). When the device is not sending, *e.g.*, receiving, the receiving device's terminators are turned off to reduce the load on the bus and power dissipation of the bus. The patent was originally assigned to Motorola, Inc., which subsequently assigned the patent to Freescale. *See* JX-3; JX-4. The '455 patent has 29 claims, of which claims 9 and 10 are asserted against Zoran and MediaTek.

C. Products at Issue

Freescale accused the following MediaTek products of infringing claims 9 and 10 of the '455 patent: [

] (collectively "the Accused MediaTek Products"). ID at 3, 72.

Freescale accused three groupings of Zoran products of infringing claims 9 and 10 of the '455 patent. Group I consists of [

] (collectively "Accused Zoran Resistor Termination Products"); Group II consists of [

] (where Groups II and II are collectively "Accused Zoran Hybrid Termination Products"). *Id.* The ALJ found that Freescale is precluded under the doctrine of issue preclusion from asserting infringement of claims 9 and 10 of the '455 patent against the following eight Zoran chip models that were specifically adjudicated in a previous investigation involving Freescale and Zoran's products, namely *Certain Integrated Circuits, Chipsets, and Products Containing Same Including Televisions, Media Players, and Cameras*, Inv. No. 337-TA-709 ("*Integrated Circuits I*"): ZR3977OBGCF; ZR39772HGCF-B; ZR39775HGCF-B; ZR39775HGCF-TC; ZR39775HGCF-TC-LP; ZR39785HGCF-B; ZR39787HGCF; and ZR39787HGCF-LP. ID at 65.[2] The Commission determined not to review this finding. *See* Notice of Review In Part at 3.

II. STANDARD OF REVIEW

Once the Commission determines to review an initial determination, its review is conducted *de novo*. *Certain Polyethylene Terephthalate Yarn and Prods. Containing Same*, Inv. No. 337-TA-457, Comm'n Op. at 9 (June 18, 2002). Upon review, the "Commission has 'all the powers which it would have in making the initial determination,' except where the issues are limited on notice or by rule." *Certain Flash Memory Circuits and Prods. Containing Same,* Inv. No. 337-TA-382, USITC Pub. 3046, Comm'n Op. at 9-10 (July 1997) (quoting *Certain Acid-Washed Denim Garments and Accessories,* Inv. No. 337-TA-324, Comm'n Op. at 5 (Nov. 1992)). Commission practice in this regard is consistent with the Administrative Procedure Act. *Certain EPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices and*

[2] All of the Zoran chips that the ID finds precluded are from Group I of the Zoran Resistor Termination Products.

Prods. Containing Same, Inv. No. 337-TA-395, Comm'n Op. at 6 (Dec. 11, 2000) ("*EPROM*"); *see also* 5 U.S.C. § 557(b).

Upon review, "the Commission may affirm, reverse, modify, set aside or remand for further proceedings, in whole or in part, the initial determination of the administrative law judge. The Commission may also make any findings or conclusions that in its judgment are proper based on the record in the proceeding." 19 C.F.R. § 210.45. This rule reflects the fact that the Commission is not an appellate court, but is the body responsible for making the final agency decision. On appeal, only the Commission's final decision is at issue. *See EPROM* at 6, citing *Fischer & Porter Co. v. U.S. Int'l Trade Comm'n*, 831 F.2d 1574, 1576-77 (Fed. Cir. 1987).

III. DISCUSSION

A. Obviousness In View Of Kuboki

Under 35 U.S.C. § 103(a), a patent is valid unless "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a). The ultimate question of obviousness is a question of law, but "it is well understood that there are factual issues underlying the ultimate obviousness decision." *Richardson-Vicks Inc. v. Upjohn Co.*, 122 F.3d 1476, 1479 (Fed. Cir. 1997).

Once claims have been properly construed, "[t]he second step in an obviousness inquiry is to determine whether the claimed invention would have been obvious as a legal matter, based on underlying factual inquiries including: (1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art;

and (4) secondary considerations of non-obviousness." *Smiths Indus. Med. Sys., Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1354 (Fed. Cir. 1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966)). The Federal Circuit has historically required that, in order to prove obviousness, the patent challenger must demonstrate, by clear and convincing evidence, that there is a "teaching, suggestion, or motivation to combine." The Supreme Court, however, rejected this "rigid approach" in *KSR Int'l Co. v. Teleflex Inc.*:

> The obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. The diversity of inventive pursuits and of modern technology counsels against limiting the analysis in this way. In many fields it may be that there is little discussion of obvious techniques or combinations, and it often may be the case that market demand, rather than scientific literature, will drive design trends. Granting patent protection to an advance that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility.

KSR Int'l Co. v. Teleflex Inc., 500 U.S. 398, 402 (2007).

Since *KSR* was decided, the Federal Circuit has announced that, where a patent challenger contends that a patent is invalid for obviousness based on a combination of prior art references, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, . . . and would have had a reasonable expectation of success in doing so." *PharmaStem Therapeutics, Inc. v. Viacell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007).

In addition to demonstrating that a reason exists to combine prior art references, the challenger must demonstrate that the combination of prior art references discloses all of the limitations of the claims. *Hearing Components, Inc. v. Shure Inc.*, 600 F.3d 1357, 1373-1374

(Fed. Cir. 2010) (upholding finding of non-obviousness based on the fact that there was substantial evidence that the asserted combination of references failed to disclose a claim limitation); *Velander v. Garner*, 348 F.3d 1359, 1363 (Fed. Cir. 2003) (explaining that a requirement for a finding of obviousness is that "all the elements of an invention are found in a combination of prior art references").

"Secondary considerations," also referred to as "objective indicia of non-obviousness," such as "commercial success, long felt but unsolved needs, failure of others, etc." may be used to understand the origin of the subject matter at issue, and may be relevant as indicia of obviousness or non-obviousness. *Graham*, 383 U.S. at 17- 18. Secondary considerations may also include copying by others, prior art teaching away, and professional acclaim. *See Perkin-Elmer Corp. v. Computervision Corp.*, 732 F.2d 888, 894 (Fed. Cir. 1984), cert. denied, 469 U.S. 857 (1984). Evidence of "secondary considerations," must be considered in evaluating the obviousness of a claimed invention, but the existence of such evidence does not control the obviousness determination. In order to accord objective evidence substantial weight, its proponent must establish a nexus between the evidence and the merits of the claimed invention, which is generally made out "when the patentee shows both that there is commercial success, and that the thing (product or method) that is commercially successful is the invention disclosed and claimed in the patent." *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995). But secondary considerations, such as commercial success, will not necessarily dislodge a determination of obviousness based on an analysis of the prior art. *See KSR*, 500 U.S. at 426 (commercial success did not alter conclusion of obviousness). A court must consider all of the evidence under the *Graham* factors before reaching a decision on obviousness. *Richardson-Vicks*,

122 F.3d at 1483-84.

The ID finds that claims 9 and 10 of the '455 patent are obvious in view of Gist combined with the knowledge of one of ordinary skill in the art and/or Kuboki. ID at 54. The ID also finds that the '455 patent is obvious in view of Kuboki in combination with the knowledge of one of ordinary skill in the art and/or Gist. ID at 58. The Commission did not review the ID's findings that the asserted claims are obvious in view of Gist combined with the knowledge of one of ordinary skill in the art. However, since our discussion concerning Kuboki involves analysis of this knowledge, we will briefly discuss the ID's findings on this issue.

With respect to the Gist reference, Respondents contended before the ALJ that "it would have been obvious to one of ordinary skill in the art to include the processor in the same IC package as the bus termination circuitry." ID at 46. Specifically, Respondent asserted that "at the time of the filing of the '455 patent, there was a long-standing, industry-wide trend toward integrating more and more functionality and circuitry onto a single chip," a point with which Respondents noted that Freescale's expert, Dr. Subramanian, agreed. *Id.* (citing Subramanian, Tr. at 656:2-7). Respondents further claimed that "microprocessors with on-chip bus termination circuits were already known in the art" and, thus, "a person or ordinary skill in the art would have considered it obvious to integrate the CPU and the dynamic termination circuitry of Gist." ID at 46-47.

The ALJ found that the testimony of both parties' experts show that "one of ordinary skill in the art at the time of the filing of the '455 patent would have found it obvious to integrate the processor and the bus termination circuitry of Gist on a single chip." ID at 49-50 (citing RX-1C at Q. 306, 309; Subramanian, Tr. at 656:2-7); *see also id.* at 52 (citing Subramanian, Tr. at

614:16-25, 617:4-8 (admitting that "[m]icroprocessors with on-chip bus termination circuits were [] known before the '455 patent[.]"). Specifically, the ALJ noted Dr. Knox' testimony regarding the benefits of single chip integration, namely "reduced size, reduced costs, reduced power consumption, and increased speed[,]" and that "one of ordinary skill in the art would have had a reasonable expectation of success in integrating the processor and bus termination circuitry of Gist on a single chip, as 'integration of multiple functionalities into a single integrated circuit was routinely practiced in the industry.'" ID at 50 (citing RX-1C at Q. 310, 312-15. The ALJ also credited Dr. Knox' reliance on an April 1992 IEEE article, concerning the trend towards chip integration, in finding that "one of ordinary skill in the art would be motivated to integrate the data processor and bus termination circuitry of Gist onto a single chip." *Id.* (citing RX-1C at Q. 149; RX-31 (IEEE article) at 52-53).

With respect to the teachings of the Kuboki reference, the ALJ noted that the parties disputed whether Kuboki discloses "[a] data processor within an integrated circuit package" that contains "a plurality of bus termination circuits," meaning a data processor and bus termination circuits on a single chip, and the limitation "a plurality of external pins" and "a plurality of bus termination circuits." ID at 41. Although he concluded that Kuboki does not anticipate claims 9 and 10 of the '455 patent, the ALJ found that Kuboki does explicitly disclose the limitation "a microprocessor with on-chip dynamic bus termination circuitry." *Id.*; *see also* ID at 51. Specifically, the ALJ noted that "Kuboki discloses nine differing embodiments of termination circuitry" as well as "a '[m]icroprocessor incorporating any one of the first through the ninth device as the input/output interface.'" ID at 41 (citing RX-5 (Kuboki) at ¶¶ 7-16, 39). The ALJ found that this language discloses "a single circuit including both a processor and termination

circuitry," crediting Dr. Knox's testimony that "since a microprocessor is itself an integrated circuit, the only logical reading is that Kuboki teaches a microprocessor with on-chip dynamic termination circuitry." *Id.* (citing RX-1C at Q. 376, 380).

The ALJ found that "[b]oth Kuboki and Gist are related to the same subject matter, namely dynamic bus termination circuitry . . . [t]hus, it would be natural for one of ordinary skill in the art to look to the teachings of Kuboki to modify the structure of Gist to integrate the processor and bus termination circuitry." *Id.* (citing RX-1C at Q. 457). The ALJ found that Freescale's argument that there were technological concerns that taught against single-chip integration "miss the mark" because "[t]he technical and/or financial problems [regarding] incorporating the claimed invention into a commercial product do not negate the fact that a prior art reference expressly discloses incorporating bus termination circuitry on a microprocessor." ID at 52.

With respect to the obviousness of claim 9 in view of Kuboki, the ALJ found that, as for the missing element of Kuboki – "a plurality of external pins" and "a plurality of bus termination circuits" – Respondents' expert, Dr. Knox, opined that "'[a] parallel data bus with multiple lines was a standard feature for high performance microprocessors in 1993[,]'" such as the microprocessor disclosed by Kuboki, and that "use of a parallel data bus with multiple lines would require the use of a plurality of external pins, one for each data line." ID at 56-57 (citing RX-1C at Q. 410, 412).[3] In particular, the ALJ noted Dr. Knox' testimony that "it would have

[3] Although Freescale did not request review of the ALJ's findings concerning the limitations "a plurality of external pins" and "a plurality of bus termination circuits," we recite them here by way of background for our discussion below.

been a matter of routine design choice to replicate the bus termination circuitry shown in Figure 4 [of Kuboki] for each data line, thereby resulting in a plurality of bus termination circuits." *Id.* (citing RX-1C at Q. 413; *see also* Q. 416 (stating that "bus I/O interfaces are module, and are generally obtained by replicating a bus I/O cell for a single data line."). The ALJ further noted Dr. Knox' testimony that "Gist teaches the use of bus termination circuitry in the context of a parallel data bus." ID at 57 (citing RX-1C at Q. 453-454, 459-460). Dr. Knox opined that "one of ordinary skill in the art would have been motivated to make this modification of Kuboki because use of a parallel bus with multiple data lines increases the data transmission rate of the bus." *Id.* (citing RX-1C at Q. 417-418). The ALJ found that Freescale's expert, Dr. Subramanian, failed to rebut Dr. Knox's testimony. ID at 57-58 (citing CX-408 at Q. 151).[4]

Respondents similarly argued before the ALJ that "to the extent that Kuboki is determined not to disclose a processor and termination circuitry integrated onto one integrated circuit, it would have been obvious to one of ordinary skill in the art that the processor and termination circuitry of Kuboki could be integrated." ID at 54. Respondents further asserted that "to the extent that Kuboki is found to only disclose a single termination circuit for a single pin, it would have been obvious to one of ordinary skill in the art to implement the teachings of Kuboki in microprocessor technology using a parallel data bus and, thus, including multiple pins and multiple bus termination circuits . . . [or] to combine Kuboki and Gist to use the bus termination circuitry of Kuboki with the parallel bus of Gist." *Id.* The ALJ noted, however, that he explicitly found, in discussing anticipation, that "Kuboki clearly discloses the limitation '[a]

[4] There was no dispute that either Gist or Kuboki discloses the additional limitations of claim 10 of the '455 patent. ID at 53-54, 58.

data processor within an integrated circuit package' with integrated bus termination circuitry." ID at 56.[5]

Although we agree with the ALJ that Kuboki in combination with the knowledge of one of ordinary skill in the art renders obvious claims 9 and 10 of the '455 patent, we do so for different reasons than those discussed in the ID. In particular, while we agree that the claim limitations "a plurality of external pins" and "a plurality of bus termination circuits" would have been obvious in light of the knowledge of one of ordinary skill in the art (*see* ID at 56-58), we find that the Kuboki reference does not disclose the claim limitation "[a] data processor within an integrated circuit package comprising: . . . a plurality of bus termination circuits."

The relevant passages of Kuboki are as follows:

> *Microprocessor incorporating* the semiconductor integrated circuit device set forth in any of claims 1 through 9 as the input/output interface.

RX-5 at Claim 10 (emphasis added);

> *Microcomputer incorporating* the semiconductor integrated circuit device set forth in any of claims 1 through 9 as the input/output interface.

RX-5 at Claim 11 (emphasis added);

> (FIELD OF INDUSTRIAL APPLICATION) This invention relates to a semiconductor integrated circuit device, particularly to a semiconductor integrated circuit device ideally suited to measuring the impedance matching between input/output interfaces when transmitting signals via input/output interfaces, and to *a microprocessor and microcomputer that* ***uses*** *this device.*

RX-5 at ¶ 1 (emphasis added);

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[5] The Commission did not review the ID's findings concerning secondary considerations. *See* ID at 60-62; Notice of Review In Part at 3.

> *Microprocessor incorporating* any one of the first through the ninth device as the input/output interface.

RX-5 at ¶ 16 (emphasis added);

> *Microcomputer incorporating* any one of the first through the ninth device as the input/output interface.

RX-5 at ¶ 17 (emphasis added);

> Although semiconductor integrated circuit devices were described in each of the aforesaid embodiments, the same effect as the aforesaid embodiments can be obtained by *using these devices to constitute a microprocessor or microcomputer*.

RX-5 at ¶ 39. The ID finds that this language provides an "unambiguous disclosure of a microprocessor with on-chip dynamic bus termination circuitry." ID at 51 (citing RX-5 (Kuboki); RX-1C at Q. 376, 380). The evidence shows, however, that the issue is not as straightforward as might appear at first glance.

The dispute concerns Kuboki's use of both the terms "microprocessor," which may refer to a single chip, and "microcomputer," which by definition is almost never incorporated on a single chip because it encompasses the many devices necessary for the microcomputer to operate. *See* CX-408C (Subramanian Rebuttal Witness Statement ("RWS")) at Q. 126. We note, however, that the relevant portion of Kuboki is not the disclosure concerning a "microcomputer." Rather, it is the disclosure concerning a "microprocessor." Kuboki teaches a "microprocessor" that not only "uses" the disclosed bus termination circuitry (*see* RX-5 at ¶ 1) but "incorporates" (*see* RX-5 at Claim 10, ¶ 16) the circuitry and that the circuitry is used to "constitute" a "microprocessor" (*see* RX-5 at ¶ 39). While the use of the term "incorporate" and "constitute" in the context of a multi-chip device like a microcomputer may mean that the bus termination circuitry is one of the many chips used to make up the microcomputer, it does not need to have

that same meaning in reference to a single device.

This understanding, however, does not resolve the question. In particular, Freescale's expert, Dr. Subramanian, acknowledged that a microprocessor need not, in fact, be implemented on a single chip or, in the language of claim 9 of the '455 patent, "within an integrated circuit package." Specifically, he testified as follows:

> As I discussed earlier, there is absolutely no necessity that all microprocessor functionality be incorporated within a single package, and indeed, even today, structures such as de-coupling capacitors, etc., are routinely placed off-chip and outside the package.

CX-408C at Q. 126. As such, while the language of Kuboki strongly suggests the incorporation of a microprocessor and bus termination circuitry into a single package, too much ambiguity remains to allow us to find that Kuboki necessarily discloses a single integrated circuit that includes both a processor and termination circuitry. As such, we find that Kuboki does not disclose by clear and convincing evidence the "[a] data processor within an integrated circuit package comprising: . . . a plurality of bus termination circuits" limitation of claim 9 of the '455 patent.

Although we find that Kuboki does not sufficiently disclose the limitation "[a] data processor within an integrated circuit package comprising: . . . a plurality of bus termination circuits" of claim 9, we adopted without review the ID's finding that it would have been obvious to one of ordinary skill in the art to integrate a data processor with bus termination circuitry on the same chip. *See* ID at 49-50; Notice of Review In Part at 3. As such, we find that Kuboki in combination with the knowledge of one of ordinary skill in the art renders obvious claims 9 and 10 of the '455 patent with respect to the limitation "[a] data processor within an integrated circuit

package comprising: . . . a plurality of bus termination circuits" of claim 9. Moreover, because, as the ID finds, Gist discloses the limitations "a plurality of external pins" and "a plurality of bus termination circuits" (ID at 57), we also find that Kuboki in combination with Gist and the knowledge of one of ordinary skill in the art renders obvious claims 9 and 10 of the '455 patent.

B. Infringement

Unfair acts under section 337 include "all forms of infringement, including direct, contributory, and induced infringement." *Certain Home Vacuum Packaging Machines*, Inv. No. 337-TA-496, Order No. 44, 2004 ITC LEXIS 202 * 2, n.2 (Mar. 3, 2004). To establish infringement, there must be a preponderance of evidence. *See Creative Compounds*, 651 F.3d at 1314. A determination of patent infringement encompasses a two-step analysis. *Advanced Cardiovascular Sys., Inc. v. Scimed Life Sys., Inc.*, 261 F.3d 1329, 1336 (Fed. Cir. 2001) ("*Scimed*"). First, the court determines the scope and meaning of the patent claims asserted, and then the properly construed claims are compared to the allegedly infringing device. *Id.* "Literal infringement of a claim exists when each of the claim limitations reads on, or in other words is found in, the accused device." *Allen Eng. Corp. v. Bartell Indus.*, 299 F.3d 1336, 1345 (Fed. Cir. 2002). Direct infringement includes the making, using, selling, offering for sale and importing into the United States an infringing product, without authority. 35 U.S.C. § 271(a). To prove direct infringement, the plaintiff must establish by a preponderance of the evidence that one or more claims of the patent read on the accused device either literally or under the doctrine of equivalents ("DOE"). *Scimed*, 261 F.3d at 1336.

Under DOE, "a product or process that does not literally infringe upon the express terms of a patent claim may nonetheless be found to infringe if there is equivalence between the

elements of the accused product or process and the claimed elements of the patented invention." *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 21 (1997). Equivalency may be determined using the "triple identity test" and thus "focusing on the function served by a particular claim element, the way that element serves that function, and the result . . . obtained by that element. . . ." *Id.* at 39. Regardless of the linguistic framework of the test used, the "essential inquiry" is: "[d]oes the accused product or process contain elements identical or equivalent to each claimed element of the patented invention?" *Id.* at 40.

Freescale argued before the ALJ that "each of the [Accused] Zoran Hybrid Termination Products [ ] ID at 112. (citing RX-218C (Herzen RWS) at Q. 97; RX-219C (Auld RWS) at Q. 111; CX-194C at 1; CX-276C at 1; CX-401C (Subramanian Direct Witness Statement) at Q. 211-14; JX-30C; JX-53C). Freescale asserted that "[ ], as shown in JX-30C at ZCO 1047 and JX-53C at ZCO 1269." ID at 115 (citing CX-401C at Q.246-47). Freescale further asserted that "the termination circuitry in the bus termination circuit [ ]." *Id.* (citing JX-7C (Auld Dep.) at 68:20-69:5; JX-30C at ZCO 1048; JX-53C at ZCO 1272; JX-7C at 68:20-69:5). Freescale further asserted that "[ ]." ID at 118-119 (citing JX-7C at 76:18-78:9; CX-401C at Q. 227-28; JX-30C at ZCO 1048; JX-53C at ZCO 1272; *see* CDX-4C.13 (Group II) and CDX-4C.20 (Group III) - annotated schematics of [ ].

With respect to the limitation "a conductor coupled to each input of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal, wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus," Freescale accused "[

]" as the claimed "conductors." ID at 118 (citing CX-401C at Q. 227, 251.) Freescale claimed that "[

]." *Id.* (citing Auld, Tr. at 180:15-183:10; JX-7C at 71:12-72:8, 74:13-76:13). Freescale asserted that "[

]." ID at 115-116. Freescale argued, therefore, that "[

]." ID at 116 (citing CX-401C at Q. 222, 246). Freescale further asserted that "in addition to [

][which] set the amount of termination impedance. *Id.* (citing JX-7C at 73:8-24, 76:18-78:9). Freescale asserted that the accused "control signals, when

asserted, couple at least one circuit component, a transistor and one or more resistors, to the bus through the [ ]." ID at 118 (citing Auld, Tr. at 180:15-183:10; JX-30C at ZCO 1048). Freescale further asserted that "when these control signals are deasserted, these circuit components are decoupled from the bus." *Id.*

The ID finds that Motorola failed to show by a preponderance of the evidence that the Accused Zoran Hybrid Termination Products satisfy the "control signal, when asserted . . . when deasserted" limitation of claim 9 of the '455 patent. ID at 143.[6] Although the ALJ apparently agreed that [ ] in JX-30C and JX-53C is a "bus termination circuit," he found, with respect to the limitation at issue, that Freescale failed to "sufficiently link the assertion or deassertion of the accused control signals [ ] with the coupling or decoupling of circuit components to say that one '***allows***' the other." ID at 154 (emphasis in original). Specifically, the ALJ found that, while "[t]he accused bus termination circuit receives [the accused control signals] as input signals[,]" the [

] respectively. ID at 154-155 (citing JX-30C at ZCO 1047, 1048; JX-53C at ZCO 1262, 1272). The ALJ noted Freescale's reliance on Zoran's witness, Mr. Auld, to show a link between the [

]. ID at 155. In particular, Freescale cited Mr. Auld's testimony that "[

[6] The ALJ noted that Zoran and Freescale agree that all of the Accused Zoran Hybrid Termination Products share the same interface circuitry and may be treated together for purposes of the infringement analysis. ID at 144.

]." *Id.* (emphasis in original) (citing Auld, Tr. at 181:5-182:8; JX-7C (Auld Dep.) at 73:17-24). The ALJ found, however, that Freescale's argument that "a signal used 'in combination with other signals,' or a signal that contributes 'in part,' to coupling circuitry" is insufficient to satisfy the disputed claim limitation. *Id.* The ALJ found that "Freescale imposes no limits on how insignificant the contributed 'part' can be, or how many other signals can be used in combination with the alleged 'control signal,' and still meet this limitation." *Id.* The ALJ stated that "[a] plain and ordinary reading of [the term] 'allows' [in claim 9] does not permit such an attenuated relationship between the accused control signal and whether circuitry is coupled to or decoupled from the bus." *Id.* The ALJ also found that "nothing in the intrinsic record supports Freescale's position[.]" *Id.*

We agree with the ALJ that the evidence does support by a preponderance of the evidence a conclusion that that accused signals [ ] signals satisfy the limitation the "control signal, when asserted . . . when deasserted" limitation of claim 9 of the '455 patent. We find, however, that the ALJ's finding is supported for reasons in addition to those articulated in the ID.

The Accused Zoran Hybrid Termination Products are shown in exhibits JX-30C (Group II) and JX-53C (Group III). [7] Freescale accuses block [ ] as the "bus termination circuit" of claim 9 of the '455 patent. ID at 115. Specifically, block [

[7] The parties agree that the Group II and Group III products operate similarly. ID at 102. As such, we will refer to the schematics that are clearest from either Group II or Group III.

]. *Id.* The arrangement of components in block

is shown in the schematics JX-30C at ZCO 1047 (Group II) and JX-53C at ZCO 1269 (Group III. The [ ] is shown in the s schematics JX-30C at ZCO 1048 (Group II) and JX-53C at ZCO 1272 (Group III) as follows:

[

]

RDX-10-14C (showing JX-30C at ZCO 1048).

Zoran corporate witness, Mr. Auld, testified at his deposition that the unasserted signal [ ] in the Accused

Zoran Hybrid Termination Products.[8] JX-7C (Auld Dep.) at 114:20-115:2. He explained that the [

]." *Id.* at 161:11-23.

So, while the accused signals [

](*see* JX-7C at 72:3-8) and the accused signals [

](*see* JX-7C at 71:18-23), without the signal [

] would not know whether it was in input mode or termination mode in the first place. As a result, without assertion of the [

] – will not signal to the termination circuits that they should turn on.

We, therefore, affirm the ID's finding that Freescale has failed to show that the Accused Zoran Hybrid Termination Circuits infringe claims 9 and 10 of the '455 patent for both the reasons stated in the ID and for the additional reasons discussed above.

C. Domestic Industry: Economic Prong

Sections 337(a)(2) and (3) set forth the domestic industry requirement:

> **(2)** Subparagraphs (B), (C), (D), and (E) of paragraph (1) apply only if an industry in the United States, relating to the articles protected by the patent, copyright, trademark, mask work, or design concerned, exists or is in the process of being established.
>
> **(3)** For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark, mask work, or design concerned—

[8] The signal is shown, for example, in exhibit JC-53C at 1272 at near the bottom left of the figure.

> **(A)** significant investment in plant and equipment;
>
> **(B)** significant employment of labor or capital; or
>
> **(C)** substantial investment in its exploitation, including engineering, research and development, or licensing.

19 U.S.C. §§ 1337(a)(2) and (3).

The economic prong of the domestic industry requirement is satisfied by meeting the criteria of any one of the three factors listed in sections 337(a)(3) above. When a complainant seeks to satisfy the domestic industry requirement through its investments in licensing under section 337(a)(3)(C), the complainant must show that it has made a substantial investment in the exploitation of the asserted patent through licensing. 19 U.S.C. § 1337(a)(3)(C); *Certain Multimedia Display and Navigation Devices and Systems, Components Thereof, and Prods. Containing Same,* Inv. No. 337-TA-694, Comm'n Op. at 7-8 (Aug. 8, 2011) ("*Navigation Devices*"). In order for a particular activity to be considered "exploitation" through licensing within the meaning of the statute, the complainant must demonstrate that it: (1) relates to the asserted patent; (2) relates to licensing; and (3) occurred in the United States.[9] *Navigation Devices*, Comm'n Op. at 7-8.

Activities that meet these three requirements merit consideration in the Commission's evaluation of whether a complainant has satisfied the domestic industry requirement, but the inquiry does not end there. *Id.* Complainant must also demonstrate the extent of its investment in these activities. In the portfolio licensing context, the Commission has indicated that it

[9] Because the statute requires that investment activities satisfy all three of these requirements, the absence of any one of them will defeat complainant's attempt to rely on that activity to satisfy the domestic industry requirement. *Navigation Devices*, Comm'n Op. at 15 n.12.

considers the relative importance of the asserted patent to the licensing investment to determine to what extent the investment in the entire portfolio can be attributed to the asserted patent. *Navigation Devices*, Comm'n Op. at 8 ("Because Pioneer's activities are associated both with the asserted patents and unasserted patents, a key issue presented is the strength of the nexus between the activities and the asserted patents.").

Finally, complainant must establish that its investment in licensing the asserted patent is substantial. *Id.* The Commission has indicated that whether an investment is "substantial" may depend on:

> (1) the nature of the industry and the resources of the complainant;
>
> (2) the existence of other types of "exploitation" activities;
>
> (3) the existence of license-related "ancillary" activities;
>
> (4) whether complainant's licensing activities are continuing; and
>
> (5) whether complainant's licensing activities are the type of activities that are referenced favorably in the legislative history of section 337(a)(3)(C).

Id. at 15-16. The complainant's return on its licensing investment (or lack thereof) may also be circumstantial evidence of substantiality. *Id.* at 16.

Before the ALJ, Freescale relied on its "[

]." ID at 158 (citing CX-402C (Chastain WS) at Q. 11).

Freescale further relied on the fact that it "[

], with related salary expenses totaling approximately [ ]. ID at 158-159 (citing CX-402C at Q. 13-18, 22; CX-1C (Chastain Decl.) at ¶¶ 4-5). Freescale also noted that its "[

]." ID at 159 (citing CX-402C at Q. 24-25; CX-1C at ¶ 3).

Freescale contended that "all of these costs were related to employees and licensing efforts in the United States." *Id.* Freescale further relied on non-payroll investments of approximately [

]. ID at 173 (citing CX-402C at Q. 24-25; CX-1C at Tab A). Freescale asserted that "'[

]." *Id.* (citing CX-402C at Q. 27).

Freescale contended that it "granted licenses to the '455 patent [ ]" and that "[ ]." *Id.* (citing CX-402C at Q.37-41, 51-63; CX-1C at ¶¶ 6-7; JX-26C [ ]; CX-29C [ ]). Freescale claimed that it often [ ] and that "[

]." *Id.* (citing CX-402C at Q. 58-61, 81 [ ]. Freescale further noted that the Commission declined to review the finding on summary determination in *Integrated Circuits I* that Freescale made a substantial investment in licensing with respect to the '455 patent. *Id.* (citing CX-2C (*Integrated Circuits I*, Order No. 33); CX-3 (Commission Notice of non-review)).

Respondents argued before the ALJ that "Freescale failed to offer any evidence on any of the five factors relating to the nexus between the claimed investment and the '455 patent" that

the Commission noted in *Navigation Devices*. ID at 160 (citing Order No. 19 (denying Freescale's motion for summary determination that it satisfies the domestic industry requirement based on licensing). Specifically, Respondents asserted that Freescale conceded that it licenses the '455 patent [

]. *Id.* Respondents further asserted that "[

]" and uses its patent portfolio [

]. ID at 160-161.

Respondents also asserted that Freescale has not offered any evidence "[

]" or "[

]." ID at 161.

The IA also argued before the ALJ that Freescale failed to satisfy the domestic industry requirement based on its licensing activities. ID at 162. In addition to the arguments presented by Respondents, the IA asserted that "[

]." *Id.* The IA further argued that "[

]." *Id.* The IA also contended that "[

]." *Id.*

The ID finds that Freescale failed to demonstrate that it satisfies the domestic industry requirement for the '455 patent based on its licensing activities. ID at 163. The ALJ did find that Freescale has demonstrated a nexus between its licensing activities in general and the '455

patent. ID at 163-168. The ALJ also found, however, that "Freescale has not met its burden to demonstrate that it has made a 'substantial investment' in licensing as required by 19 U.S.C. § 1337(a)(3)(C)." ID at 176.

The ALJ noted that, for the employees that Freescale identifies as being involved in licensing operations, Freescale's corporate witness, "Mr. Chastain[,] acknowledges that [

]." ID at 171 (citing JX-16C (Chastain Dep.) at 123:4-20). The ALJ, therefore, found that "it is improper to include the employees' full salaries in the calculation when [

]." ID at 171-172. The ALJ also declined to consider Freescale's non-payroll investments, specifically, those concerning its [

]." ID at 173 (citing JX-16C at 179:4-180:8, 225:25-226:15; CX-402C at Q. 27; JX-23C (Guzaldo Dep.) at 62:22-63:7). The ALJ found that "[

]." ID at 174.

The ALJ, therefore, considered only Freescale's remaining non-payroll expenses, which amounted to [ ]. ID at 175. The ALJ found that "Freescale is a large corporation with [

]." *Id.* (citing RX-156 at 5, 35). The ALJ concluded that "[

]" and is, therefore, not substantial within the meaning of section 337(a)(3)(C). *Id* (citing *Navigation Devices* at 15 (finding that "whether an investment is substantial may depend on the industry and the size of the complainant.")

We agree with the ALJ that Freescale has failed to prove that it has made a substantial investment in the exploitation of the '455 patent through its licensing activities. We further agree with the ALJ that Freescale's [ ] should not be considered because it is not known what proportion of those costs are domestic versus foreign. We also agree that Freescale cannot rely on its payroll expenditures. Additionally, we find that Freescale failed to demonstrate how those costs relate to the asserted patent. Furthermore, we find that the ALJ should not have considered Freescale's remaining non-payroll expenses because of a similar lack of proof concerning how those expenses relate to the asserted patent.

The dispute with respect to whether Freescale has demonstrated that it has a license-based domestic industry centers on the issue of how to apportion their investments in licensing. The Commission has recently provided guidance on this issue in Certain *Semiconductor Chips and Products Containing Same*, Inv. No. 337-TA-753, Comm'n Op. at 44-51 (July 31, 2012) ("*Semiconductor Chips*"). In that case, the complainant, Rambus, Inc., asserted two groups of patent claims, the Barth patents and the Dally patents. *Id.* at 4-5. Rambus argued that it had a licensed-based domestic industry due to its investment in licensing the Barth and Dally patents. *Id.* at 44. The presiding ALJ in that investigation found that Rambus had shown that its

investment in licensing those patents was "substantial," but the Commission reversed the ALJ's determination. *Id.* In reaching the decision, the Commission assumed for purposes of its analysis that Rambus had demonstrated a nexus between the asserted patents and Rambus's license portfolios. The Commission noted, however, that "what is wanting in this investigation . . . is evidence specifically demonstrating [the] investment made in the licenses upon which Rambus relies, as opposed to overall firmwide licensing expenses." *Id.* at 47, n. 19. The Commission, therefore, concluded that the evidence Rambus presented concerning its

> total amount of licensing expenditures and total number of licensing-related employees . . . does not allow the Commission to qualitatively or quantitatively determine what portion of [Rambus's firmwide investment], or what portion of the expenses associated with the activities of . . . Rambus employees that work on the overall licensing program, could be allocated in some fashion to licensing the Dally and Barth patents.

Id. at 47.

Similar to the evidence Rambus presented in *Semiconductor Chips*, the evidence presented by Freescale here does not allow the Commission to ascertain how the '455 patent relates to its overall licensing program. Freescale offers [

]. JX16C at 58:9-11; 59:10-60:16. Freescale does not indicate the number of portfolio licenses it has entered into that actually license the '455 patent. Instead, Freescale simply put into evidence a sampling of its [

]. CX-402C at Q. 40-42. Further, Freescale's corporate witness, Mr. Chastain, did not clarify the issue. He did testify that the company has [

]. JX-16C at 22:11-17, 27:11-20. Mr. Chastain stated, however, that he was unaware of what percentage [ ] related to the various technology areas, although he speculated that the circuit design area, of which the '455 patent is a part, [ ]. *Id.* at 27:21-29:19. Although Mr. Chastain estimated that Freescale has entered into [ ], he could not detail what percentage of Freescale's licensing revenues since 2005 are attributable [ ]. *Id.*

Based on this evidence, we are left to speculate as to what percentage of Freescale's licensing investment is attributable to those licenses that include the '455 patent. Although the Commission does not require mathematical precision, it does require an adequate evidentiary basis for evaluating the level of investment for the licenses that include the '455 patent. As such, even assuming that the ID's finding of a nexus between Freescale's licensing portfolios and the '455 patents is correct, Freescale has failed to present sufficient evidence to allow us to determine what portion of its investment we should consider, and thus, to determine whether its investment is "substantial," as required by section 337(a)(3)(C).

Furthermore, although not addressed by the ALJ, we note that the payroll evidence Freescale presents is from 2011 and 2012, and thus, mostly from a time period subsequent to the filing of the Complaint in June of 2011. As the Commission noted in *Certain Video Game Systems and Controllers*, Inv. No. 337-TA-743, Commission Opinion at 4-7 (January 20, 2012) (Public Version), although there may be circumstances in which it is appropriate to look at a complainant's domestic activity subsequent to the filing of the Complaint, "as a general matter,

the only activities that are relevant to the determination of whether a domestic industry exists or is in the process of being established are those that occurred before the complaint was filed." *Id.* at 5. There is no evidence in this investigation that it is appropriate to look at Freescale's post-complaint activities. For instance, Freescale has not filed for bankruptcy since filing its Complaint, neither has any "new, relevant and timely disclosed evidence" come to light, nor does Freescale's industry appear to be "dwindling." *See, e.g., Certain Semiconductor Integrated Circuits and Products Containing the Same,* Inv. No. 337-TA-665, ID at 229-30 (Oct. 19, 2009) (examining a complainant's domestic industry where the complainant filed for bankruptcy after filing a complaint with the Commission) (unreviewed in relevant part); *Certain Electronic Devices, Including Mobile Phones, Portable Music Players, and Computers,* Inv. No. 337-TA-701, Order No. 58, at 6 (Nov. 18, 2010) (unreviewed) ("the International Trade Commission typically looks to the time a complaint is filed, but there have been a number of instances when it has been acceptable to look later in the investigation, either because of the development of new, relevant and timely disclosed evidence or because there is evidence that a complainant's domestic industry is dwindling."); *Certain Electronic Imaging Devices,* Inv. No. 337-TA-726, Order No. 18 (Feb. 7, 2011) (unreviewed) ("The Commission . . . has examined the existence of a domestic industry at various points in the investigation time line, depending on the circumstances of the case."). We further note that Freescale was formed in 2004, and that in *Integrated Circuits I,* Freescale provided information concerning its domestic industry in 2009 and 2010, which information was readily available to Freescale in this investigation. *See* CX-2C (*Integrated Circuits I,* Order No. 33). As such, we believe it is inappropriate for Freescale to rely primarily on post-complaint activity in attempting to establish its domestic industry in this

investigation.

With respect to Freescale's non-payroll costs, an analysis of these investments suffers from the same evidentiary problems as its payroll investments. Specifically, there is no evidence showing what portion of Freescale's non-payroll licensing investments have a nexus to the '455 patent. Moreover, we cannot even determine from the evidence Freescale presents what portion of its licensing investments concerns domestic versus foreign licenses. As such, we have no way to determine the amount of Freescale's investments we should consider in determining whether or not its domestic investments are substantial within the meaning of the statute.

We do recognize that Freescale has been rather successful in licensing companies in the semiconductor and electronic device industry. *See* CX-1C at Tab D (listing [

] as licensees to Freescale's portfolio that includes the '455 patent). It is difficult, however, to determine how Freescale's revenues support its claims of a domestic industry because it admits that the licenses are [

]. *See* JX-16C at 29:11-19, 47:14-21, 59:7-15, 84:1-7. Contrast this with the facts in *Certain Liquid Cristal Display Devices, Including Monitors, Televisions, and Modules and Components Thereof*, Inv. No. 337-TA-741/749, Comm'n Op. (July 6, 2012), where the Commission found that the complainant licenses its patents in discrete technology groups. *Id.* at 117-119. Freescale does not provide any such level of detail, leaving us unable to determine how much of its licensing-based revenue to credit to those licenses that are related to the '455 patent. We, therefore, find that the question of whether Freescale's investment is substantial

cannot be analyzed due to a lack of an adequate evidentiary basis.

Freescale argued in its petition for review that the ID's finding of no domestic industry is contrary to the finding of the presiding ALJ in *Integrated Circuits I.* We note, however, that Freescale's motion for summary determination of a license-based domestic industry in *Integrated Circuits I* (Order No. 33, unreviewed) was granted prior to the issuance of the Commission's opinion in *Navigation Devices.* The Commission's opinion in *Navigation Devices* laid out a comprehensive framework which was not available to former Chief Judge Luckern in *Integrated Circuits I.* As the ALJ noted in denying Freescale's motion for summary judgment in this investigation, the decision in *Integrated Circuits I* did not analyze the factors that the ALJ was required to consider under *Navigation Devices. See* Order No. 19 at 7. Moreover, we note that, while Freescale is correct that the *Navigation Devices* opinion cites Order No. 33 in *Integrated Circuits I* approvingly, the citation was in the context of how a complainant may show a nexus between its licensing activities and the asserted patent, not whether or not the Commission should fully credit payroll expenses under a "substantial investment" analysis. *See Navigation Devices* at 11, n. 7 (citing *Integrated Circuits I,* Order No. 33 as "noting that the patent-at-issue was identified to potential licensees).

Accordingly, we affirm the ID's finding that Freescale failed to establish the existence of a domestic industry based on its licensing activities with the modified analysis indicated above.

IV. CONCLUSION

For the reasons discussed above, the Commission affirms with the above modifications the ID's finding of no violation of section 337.

CORRECTED PUBLIC VERSION

By order of the Commission.

Lisa R. Barton
Acting Secretary to the Commission

Issued: October 10, 2012

CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS **337-TA-786**

CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **COMMISSION OPINION** has been served by hand upon Commission Investigative Attorney **Juan S. Cockburn** and the following parties as indicated, on **October 10, 2012**

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PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of	
CERTAIN INTEGRATED CIRCUITS, CHIPSETS, & PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS	**Inv. No. 337-TA-786**

INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION ON REMEDY AND BOND

Administrative Law Judge Robert K. Rogers, Jr.

(July 12, 2012)

Appearances:

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For the Commission Investigative Staff:

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Pursuant to the Notice of Investigation and Rule 210.42 of the Rules of Practice and Procedure of the United States International Trade Commission, this is the Administrative Law Judge's Final Initial Determination in the matter of Certain Integrated Circuits, Chipsets, & Products Containing Same Including Televisions, Investigation No. 337-TA-786.

The Administrative Law Judge hereby determines that a violation of Section 337 of the Tariff Act of 1930, as amended, has not been found in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits, chipsets, and products containing same including televisions, in connection with U.S. Patent No. 5,467,455 ("the '455 patent").

The following abbreviations may be used in this Initial Determination:

CPX	Complainant's physical exhibit
CDX	Complainant's demonstrative exhibit
CX	Complainant's exhibit
CIB	Complainant's initial post-hearing brief
CRB	Complainant's reply post-hearing brief
RPX	Respondents' physical exhibit
RDX	Respondents' demonstrative exhibit
RX	Respondents' exhibit
MIB	MediaTek's initial post-hearing brief
MRB	MediaTek's reply post-hearing brief
ZIB	Zoran's initial post-hearing brief
ZRB	Zoran's reply post-hearing brief
Dep.	Deposition
JSRCC	Joint Statement Regarding Claim Construction
JSCI	Joint Stipulation of Contested Issues
JX	Joint Exhibit
Tr.	Transcript
CPHB	Complainant's pre-hearing brief
MPHB	MediaTek's pre-hearing brief
ZPHB	Zoran's pre-hearing brief

I. BACKGROUND

A. Procedural History

On July 8, 2011, the Commission issued a Notice of Investigation in this matter to determine:

> [W]hether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain integrated circuits, chipsets, and products containing same including televisions that infringe one or more of claims 9 and 10 of [U.S. Patent No. 5,467,455], and whether an industry in the United States exists as required by subsection (a)(2) of section 337.

(*See* Notice of Investigation.) The investigation was instituted upon publication of the Notice of Investigation in the *Federal Register* on July 14, 2011. *See* 76 Fed. Reg. 41521-22 (2011). 19 CFR § 210.10(b).

The complainant is Freescale Semiconductor, Inc., 6501 William Cannon Drive West, Austin, TX 78735 ("Freescale"). The respondents are Funai Electric Co., Ltd., 7-7-1 Nakagaito, Daito, Osaka 574-0013, Japan; Funai Corporation, Inc., 201 Route 17, Suite 903, Rutherford, NJ 07070 (collectively "Funai"); MediaTek Inc., No. 1 Dusing Road, Hsinchu Science Park, Hsinchu City, Taiwan 30078 ("MediaTek"); and Zoran Corporation, 1390 Kifer Road, Sunnyvale, CA 94086 ("Zoran"). The Commission Investigative Staff of the Office of Unfair Import Investigations ("Staff") is also a party in this investigation.

On April 24, 2012, I issued Order No. 27, an Initial Determination terminating the investigation as to Funai on the basis of a consent order. On May 25, 2012, the Commission issued a Notice indicating that it would not review Order No. 27.

On May 9, 2012, I issued Order No. 31, an Initial Determination terminating the investigation as to Zoran accused products { } and MediaTek

accused products {

} On May 29, 2012, the Commission issued a Notice indicating that it would not review Order No. 31.

An evidentiary hearing in this investigation was held on May 23-25, 2012.

B. The Private Parties

1. Freescale

Freescale is a Delaware corporation with its headquarters located in Austin, Texas. (Complaint at ¶ 12.) Freescale was formed in 2004 as a result of the divestiture of the Semiconductor Products Sector of Motorola, Inc. (*Id.*) Freescale employs approximately 19,000 people in more than 20 countries, including approximately 6,000 people in the United States. (*Id.*)

2. MediaTek

MediaTek is a semiconductor company with headquarters located in Hsinchu, Taiwan. (RX-222C at Q. 8, 10.) MediaTek has research and development facilities throughout the world, including Massachusetts, California, and Texas. (*Id.* at Q. 11.)

3. Zoran

Zoran was a publicly traded company having its principal place of business in Sunnyvale, California. (Complaint at ¶ 76; Zoran Resp. to Complaint at ¶ 76.) In August 2011, CSR plc acquired Zoran by virtue of a corporate merger transaction. (RX-220C at Q. 4.) Zoran is now an indirect subsidiary of CSR plc. (*Id.* at Q. 5.)

C. Overview Of The Patent At Issue

U.S. Patent No. 5,467,455 is entitled "Data processing system and method for performing dynamic bus termination." (JX-1.) It lists James G. Gay and William B. Ledbetter, Jr. as the

inventors. (*Id.*) It was filed on November 3, 1993, and issued on November 14, 1995. (*Id.*) The Abstract of the '455 patent states:

> A data processing system and a method for performing dynamic bus signal termination uses a dynamic bus termination circuitry (14 or 16) with a device (10 or 12). The circuitry is enabled when data is incoming to the device and is disabled when data is outgoing from the device to selectively reduce unwanted signal reflection at the signal end of a bi-directional bus (17). The disabling allows the circuitry to be removed or tristated from any connection with the bus (17) when not needed (i.e., data outgoing) to reduce loading. The disabling of the termination circuitry also aids in reducing the power consumption of the part when either the bus is sitting idle or the part is in a low power mode of operation.

(JX-1 at Abstract.)

D. Products At Issue

Freescale accuses the following MediaTek products of infringing claims 9 and 10 of the '455 patent: {

} (CIB at 14-15; CX-401C at Q. 63.)

Freescale accuses three groupings of Zoran products of infringing claims 9 and 10 of the '455 patent. {

} (CIB at 33; CX-401C at Q. 178.)

II. JURISDICTION

A. Subject Matter Jurisdiction

The complaint alleges that MediaTek and Zoran have violated Subsection 337(a)(1)(B) by the importation and sale of products that infringe the asserted patent. I find that MediaTek imports into the United States, sells for importation, or sells within the United States after importation products that Freescale has accused of infringement in this investigation. (CX-410C.) I find that Zoran imports into the United States, sells for importation, or sells within the United States after importation products that Freescale has accused of infringement in this investigation. (CX-274C.) Thus, I find that the Commission has subject matter jurisdiction over this investigation under Section 337 of the Tariff Act of 1930. *See Amgen, Inc. v. United States Int'l Trade Comm'n*, 902 F.2d 1532, 1536 (Fed. Cir. 1990).

B. Personal Jurisdiction

MediaTek and Zoran each responded to the complaint and notice of investigation, participated in the investigation, made an appearance at the hearing, and submitted post-hearing briefs. Thus, I find that MediaTek and Zoran submitted to the personal jurisdiction of the Commission. *See Certain Miniature Hacksaws*, Inv. No. 337-TA-237, Initial Determination, 1986 WL 379287 (October 15, 1986).

C. In Rem Jurisdiction

The Commission has *in rem* jurisdiction over the products at issue by virtue of the finding that accused products have been imported into the United States. *See Sealed Air Corp. v. United States Int'l Trade Comm'n*, 645 F.2d 976, 985 (C.C.P.A. 1981).

III. CLAIM CONSTRUCTION

A. Applicable Law

"An infringement analysis entails two steps. The first step is determining the meaning and scope of the patent claims asserted to be infringed. The second step is comparing the properly construed claims to the device accused of infringing." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*), *aff'd*, 517 U.S. 370 (1996) (citation omitted). Claim construction "is a matter of law exclusively for the court." *Id.* at 970-71. "The construction of claims is simply a way of elaborating the normally terse claim language in order to understand and explain, but not to change, the scope of the claims." *Embrex, Inc. v. Serv. Eng'g Corp.*, 216 F.3d 1343, 1347 (Fed. Cir. 2000). "[O]nly those [claim] terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy." *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Claim construction focuses on the intrinsic evidence, which consists of the claims themselves, the specification, and the prosecution history. *See generally Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). The Federal Circuit in *Phillips* explained that in construing terms, courts must analyze each of these components to determine the "ordinary and customary meaning of a claim term," which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1313.

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" *Id.* at 1312 (citations omitted). "Quite apart from the written description and the prosecution history, the claims themselves provide substantial guidance as to the meaning of particular claim terms." *Id.* at 1314. For example, "the context in which a term is used in the asserted claim can be highly instructive," and "[o]ther

claims of the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment as to the meaning of a claim term." *Id.*

"[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id.* (citation omitted). "The longstanding difficulty is the contrasting nature of the axioms that (a) a claim must be read in view of the specification and (b) a court may not read a limitation into a claim from the specification." *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004). The Federal Circuit has explained that there are certain instances when the specification may limit the meaning of the claim language:

> [O]ur cases recognize that the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs. In other cases, the specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor. In that instance as well, the inventor has dictated the correct claim scope, and the inventor's intention, as expressed in the specification, is regarded as dispositive.

Phillips, 415 F.3d at 1316.

In addition to the claims and the specification, the prosecution history should be examined if in evidence. "The prosecution history…consists of the complete record of the proceedings before the PTO and includes the prior art cited during the examination of the patent. Like the specification, the prosecution history provides evidence of how the PTO and the inventor understood the patent." *Id.* at 1317 (citation omitted). "[T]he prosecution history can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id.*

If the intrinsic evidence does not establish the meaning of a claim, then extrinsic evidence may be considered. Extrinsic evidence consists of all evidence external to the patent and the prosecution history, including dictionaries, inventor testimony, expert testimony and learned treatises. *Id.* at 1317. Extrinsic evidence is generally viewed "as less reliable than the patent and its prosecution history in determining how to read claim terms[.]" *Id.* at 1318. "The court may receive extrinsic evidence to educate itself about the invention and the relevant technology, but the court may not use extrinsic evidence to arrive at a claim construction that is clearly at odds with the construction mandated by the intrinsic evidence." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 977 (Fed. Cir. 1999).

B. The '455 patent

1. Level of Ordinary Skill in the Art

Freescale's expert Dr. Subramanian opined that a person of ordinary skill in the art would have had a Bachelor's degree in electrical engineering or equivalent, with a few years of experience, particularly focused on issues related to memories and memory systems. (CX-401C at Q. 8.)

Respondents' expert Dr. Knox opined that a person of ordinary skill in the art would have had at least a Bachelor's degree in electrical engineering or the equivalent, with a few years of experience on issues related to the design of integrated circuits, computer hardware and software, and/or microprocessors and memories as of the relevant priority date. (RX-1C at Q. 189.) Dr. Knox believes that a deficiency in one of these criteria could be compensated for by more experience or a higher degree. (*Id.*)

Zoran's expert Dr. Von Herzen opined that a person of ordinary skill in the art would have had a Bachelor's degree in computer science or electrical engineering, with several years of relevant experience including bus standards and termination techniques. (RX-218C at Q. 52.)

The experts' opinions regarding level of ordinary skill in the art are all very similar. I find that a person of ordinary skill in the art would have had a Bachelor's degree in electrical engineering or the equivalent, plus at least two years of work experience related to the design of integrated circuits, including experience in bus standards and termination techniques. I find that this level of experience properly tracks the '455 patent, which generally concerns integrated circuit design, and more specifically concerns the design of bus termination circuits for use in integrated circuits. (*See* JX-1 at 1:1-2:11.)

2. Agreed-Upon Constructions

The parties have agreed on the following constructions:

Term	Construction
"couple"	"to electrically connect [to]"
"decouple"	"to electrically disconnect [from]"
"execution unit"	"a portion of an integrated circuit that executes commands or instructions"
"bus termination circuit"	"circuitry for signal termination that is selectively enabled or disabled in response to a control signal whose assertion is based, at least in part, on the direction of data signals on the bus"

These agreed-upon constructions shall be applied in this Initial Determination.

3. "A Conductor Coupled to Each Input of Each of the Bus Termination Circuits in the Plurality of Bus Termination Circuits"

The phrase "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits" appears in asserted claim 9.

Freescale's Position: Freescale contends that no construction is necessary, and that the plain and ordinary meaning applies.

Freescale argues that Respondents and Staff improperly seek to import two additional limitations into the claim language through their proposed constructions. Freescale claims that Respondents and Staff seek to require that "a conductor" be limited to a common or single conductor. Freescale asserts that this position goes against the well-settled rule in claim construction that "a" means "one or more." According to Freescale, Respondents fail to point to any intrinsic evidence that evinces a clear intent to deviate from the ordinary rule that "a" means "one or more."

Freescale notes that Dr. Subramanian testified that under Respondents' claim construction, all control signals would be electrically connected to a common conductor, which negates the ability to have separate control signals. (Citing CX-401C at Q. 55; CX-408C at Q. 61.) Freescale argues that such a nonsensical construction cannot be correct.

Freescale notes that Respondents argue that because claim 9 refers to a "plurality" of other claim elements but does not refer to a plurality of conductor, then "a conductor" should be interpreted to mean a single conductor. (Citing RX-1C at Q. 202.) Freescale argues that the claim's use of the term "plurality" when referring to other elements does not dictate that "a conductor" is limited to a single conductor. (Citing *Free Motion Fitness, Inc. v. Cybex, Int'l, Inc.*, 423 F.3d 1343, 1345 (Fed. Cir. 2005).)

Freescale notes that Respondents point to claim language referring to "the control signal" and conclude that such language refers to "a single control signal," therefore requiring the same conductor to carry the single control signal. (Citing RX-1C at Q. 203.) Freescale argues that the use of the definite article "the" to refer back to "a" does not implicate the singular. (Citing *Baldwin Graphic Systems, Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1343 (Fed. Cir. 2008).)

Freescale argues that the specification expressly teaches embodiments in which multiple conductors are coupled to each input of each of the bus termination circuits. Freescale states that Dr. Subramanian testified that both Figure 5 and Figure 6 show the use of more than one conductor. (Citing Tr. at 325:20-25, 326:24-327:12, 337:6-9; JX-1 at Figs. 5-6.) Freescale further states that the specification expressly states that the bus termination circuit can be connected to other components via at least one conductor. (Citing JX-1 at 4:15-17.)

Freescale claims that Respondents' reliance on the inventor's testimony is unpersuasive because inventor testimony is of little probative value with respect to claim construction. Freescale also claims that the testimony at issue is referring only to the embodiment depicted in Figure 1, not the invention as a whole. (Citing JX-15C at 127:1-129:7.)

Freescale states that Respondents apparently intend to use their proposed construction for the "a conductor..." limitation to require that there be a conductor from the input of the bus termination circuit to the at least one circuit component. (Citing CX-401C at Q. 57; CX-48C at Q. 61.) Freescale argues that there is no requirement in the claim language that the claimed "conductor" be coupled with or otherwise connected to the "at least one circuit component." (Citing JX-1 at 10:42-52.) Freescale claims that the specification likewise does not impose a "continuous" conductor requirement. (Citing JX-1 at 3:64-4:50, 7:10-48, Figs. 1, 5.)

Respondents' Position: Respondents contend that "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits" means "every input of every bus termination circuit in the plurality of bus termination circuits is electrically connected to a common conductor."

Respondents note that the primary dispute is whether the "a" should be understood to mean "one" or "one or more." Respondents argue that "a conductor" should be read to mean "a

common conductor." Respondents argue that where the claim language at issue distinguishes between single and plural elements in the same claim, the singular form should be given meaning by limiting that element to a single item.

Respondents argue that in a prior investigation involving the '455 patent, Dr. Subramanian believed that "a conductor..." was limited to a single conductor. (Citing Tr. at 248:19-250:22.) According to Respondent, Dr. Subramanian could provide no explanation for his inconsistency between his position in the prior investigation and his position in this investigation. (Citing Tr. at 251:22-252:1.)

Respondents state that the testimony of named inventor James Gay confirms that the embodiment of the '455 patent use a common conductor to provide the control signal to all bus termination circuits. (Citing JX-15C at 128:17-129:7.) According to Respondents, Mr. Gay testified that one advantage to using a single conductor to control each of the bus termination circuits shown in Figure 1 is that this approach makes it easy to connect all the bus termination circuits and thus requires less circuitry. (Citing JX-15C at 130:10-131:11.) Respondents assert that Figure 1 shows a single conductor providing a single control signal for all of the bus termination circuits. (Citing RX-1C at Q. 204; Tr. at 243:15-19.) Respondents state that other embodiments, including those shown in Figures 5 and 6, also include a common conductor coupled to every one of a plurality of bus termination circuits. (Citing Tr. at 439:15-440:5, 445:13-446:6.)

Staff's Position: Staff contends that "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits" means "a single conductor connected to the input of each of the bus termination circuits."

Staff states that its proposed construction gives meaning to each word in the "a conductor" claim limitation, and it is consistent with the specification discussing the embodiments as depicted in Figures 1, 2, and 5. Staff claims that Freescale's position eliminates two instances of the word "each" in the limitation.

Staff states that when the claim expressly distinguishes between the singular and the plural, the singular element "a" should be construed as limited to only one item. (Citing *Harari v. Lee*, 656 F.3d 1331, 1341 (Fed. Cir. 2011).) Staff notes that claim 23 expressly requires different enabling signals, as opposed to the claim language of claim 9 that is limited to a common conductor. Staff contends that Figure 6 of the '455 patent supports Staff's position. (Citing JX-1 at 4:49-8:30, Fig. 6; RX-221C at Q. 25.)

Construction to be applied: "a conductor" means "one or more conductors"

The '455 patent seeks to solve the problem of signal reflection. It explains signal reflection in the following manner:

> It is known in the art that devices operating at high speeds, devices operating at high clock frequencies, and/or devices which require extremely long conductive interconnections suffer from a performance-reducing phenomenon referred to as a known and understood signal reflection or transmission line effect problem. If a zero volt signal is changed to a five volt signal, for example, on a conductor or bus which is either long in length or operating at a fast edge rate, if the bus or conductive line is not properly terminated via an impedance, the conductive line or bus will take time to settle to the 5 volt value from the 0 volt value due to one or more reflections off one or both ends of the bus.

(JX-1 at 1:12-23.)

The '455 patent states that a termination circuit may be used to reduce signal reflection:

> To reduce signal reflection and thereby improve performance, permanent resistors have been placed at the ends of uni-directional buses to reduce signal reflection. This uni-directional termination is easy to do since only one end of the bus is ever receiving data (the other end is always sending) and therefore termination of the receiving side is all that is required. Unfortunately, if the bus is idle or the part is

> in a low power mode of operation, the connected permanent resistor usually caused increased power consumption which is disadvantageous.

(JX-1 at 1:23-33.)

The '455 patent notes that in a situation where there is a bi-directional bus, use of the prior art termination circuitry creates problems related to an increased load to the bus and increased power consumption:

> In a bi-directional bus, the termination problem is enhanced because either end of the bus may either be receiving or transmitting at any time. Therefore, in the prior art, permanent resistor termination is placed at both ends of the bus and are connected regardless of whether or not they are needed. This results in an increased load to the bus and increased power consumption when the bus is placed into a low power mode of operation.

(JX-1 at 1:34-41.)

Thus, the '455 patent sets out to reduce signal reflection on a bi-directional bus while solving the problems encountered by the prior art. It solves the problem by using dynamic bus termination, which is described as follows:

> In general, the apparatus and method illustrated herein is designed to dynamically enable the proper termination inside a receiver at the end of the bi-directional bus. The proper termination is dynamically connected to the bus only when data is being received in order to reduce signal reflection on the bus (i.e. transmission line effects) and allow for a more rapid operational speed. This dynamic bus termination requires a control signal which indicates to the receiving device the current drive direction of the bus (i.e., is data being read from the device or is data being written to the device). When this control signal indicates the bus has a voltage and/or current which is being driven into the receiving device, the receiving device turns on its termination devices to dampen the incoming signal so no reflections are sent back down the bus (transmission line). When the control signal indicates the bus is not being driven into the receiving device the receiving device's terminators are turned off to reduce the load on the bus and power dissipation of the bus.

(JX-1 at 2:53-3:4.)

Claim 9 of the '455 patent recites the following:

9. A data processor within an integrated circuit package comprising:

an execution unit internal to the data processor;

a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus;

a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal; and

a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus.

(JX-1 at 10:26-52.)

The parties dispute the meaning of the claim language "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal…" The dispute is focused on whether or not there must be a common conductor for all of the bus termination circuits.

The Federal Circuit "has repeatedly emphasized that an indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.'" *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000). "That 'a' or 'an' can mean 'one or more' is best described as a rule, rather than merely as a presumption or even a convention." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008).

There is an exception to the rule. "Unless the claim is specific as to the number of elements, the article 'a' receives a singular interpretation only in ***rare circumstances*** when the patentee evinces a ***clear intent*** to so limit the article." *KCJ*, 223 F.3d at 1356 (emphasis added). The Federal Circuit has made clear that "standing alone, a disclosure of a preferred or exemplary embodiment encompassing a singular element does not disclaim a plural embodiment." *Id.*

I turn first to the claim language. The integrated circuit package of claim 9 includes a "plurality of external pins." The integrated circuit package also includes a "plurality of bus termination circuits." These elements are connected in the following manner: "one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit." Thus, each bus termination circuit is coupled to only one external pin, but each external pin may be connected to one or more bus termination circuits.

The claim then provides that "each bus termination circuit in the plurality of bus termination circuits [has] an input for receiving a control signal." The claim requires "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal." Based on this language, and the general rule that "a" or "an" in an open-ended claim means one or more, each bus termination circuit may have one or more inputs for receiving one or more control signals, and there is a conductor coupled to each of those inputs to provide the control signals. The plain language of claim demonstrates there may be one or more conductor coupled to each bus termination circuit through one or more inputs to provide one or more control signals .

Respondents assert that the claim language should be construed to mean "every input of every bus termination circuit in the plurality of bus termination circuits is electrically connected

to a common conductor." Staff similarly asserts that there is "a single conductor connected to the input of each of the bus termination circuits." These constructions are not driven by the plain language of the claims, as Respondents and Staff seek to add a "common" or "single" limitation that is not present in claim 9.

Respondents and Staff rely heavily on the fact that the phrase is question refers to "a conductor" while also referring to "bus termination circuits" and "the plurality of bus termination circuits." Respondents cite to *Harari v. Lee*, 656 F.3d 1331, 1341 (Fed. Cir. 2011) and argue that "[w]here the claim language at issue distinguishes between single and plural elements within the same claim, the selected singular form should be given meaning by limiting that element to a single item." (MIB at 8.) The claim at issue in *Harari* recited a method comprising accessing a number of control gates and a bit line to activate a number of cells. The court found that the claim expressly distinguished between the singular and the plural by reciting "accessing a number of control gates" while "accessing a bit line" to activate "a number of memory cells." *Harari*, 656 F.3d at 1341. The court thus concluded that "a bit line" was properly read as a single bit line. *Id.*

I do not find that the decision in *Harari* dictates Respondents' proposed construction. First, and most importantly, the specification of the '455 patent, as described *infra*, discloses embodiments utilizing more than one conductor for each bus termination circuit. The court in *Harari* does not state that the specification of the patent at issue disclosed an embodiment utilizing multiple bit lines. *See Harari*, 656 F.3d at 1341-1342. Second, the claim at issue in this investigation is an apparatus claim, and not a method claim. The court in *Harari* expressly noted that it reached its result in part because the claim was a method claim and not an apparatus claim: "In this case, the relevant independent claim does not recite a memory device having 'a' bit line.

Instead, it recites a *method* comprising accessing a *number* of control gates and *a* bit line to activate a *number* of cells." *Id.* at 1341 (emphasis in original).

I find that this case is more akin to *Free Motion Fitness, Inc. v. Cybex Int'l, Inc.*, 423 F.3d 1343 (Fed. Cir. 2005). Moreover, I find that *Free Motion* is distinguishable on the facts from *Harari* because it addresses an apparatus claim, and not a method claim. In *Free Motion*, the district court held that the term "a cable linking" was limited to a single cable. As the Federal Circuit recounted:

> The district court reached this construction by pointing to the patents' numerous references to a single cable ("a cable linking" and "the cable") and inferring from the patents' use of the plural in other instances "that if the patent intended more than one cable, it would have expressly indicated that by using a plural term."

Id. at 1350 (quoting *Free Motion Fitness, Inc. v. Cybex Int'l, Inc.*, 311 F. Supp. 2d 1297, 1302 (D. Utah 2003)).

The Federal Circuit reversed the district court, finding that the claim covered the use of one or more cables. *Id.* at 1350-1351. The court also rejected the idea that use of the phrase "the cable" later in the claim supported the district court's construction: "Like the words 'a' and 'an,' the word 'the' is afforded the same presumptive meaning of 'one or more' when used with the transitional phrase 'comprising.'" *Id.*

The court in *Free Motion* reached its decision even though the specification included references to the use of a single cable, explaining "[t]he references to a single cable in the specification are found in the description of the preferred embodiments, and do not evince a clear intent by the patentee to limit the article to the singular." *Free Motion*, 423 F.3d at 1350. As described *infra*, I find that the current situation is an even stronger case than the one in *Free Motion* because the '455 patent specification expressly includes embodiments using one or more conductors.

In another case addressing an apparatus claim, the Federal Circuit reversed a district court's claim construction of "an illumination apparatus" because the district court limited the claim language to a single illumination apparatus. *Scanner Techs. Corp. v. ICOS Vision Sys. Corp., N.V.*, 365 F.3d 1299, 1304-1305 (Fed. Cir. 2004). The court expressly rejected an argument that is similar to the one advanced by Respondents, namely that because the claim language calls out other limitations in the plural, but only refers to "an illumination apparatus," it means that the claim should be limited to a single illumination apparatus. *Id.* The court stated:

> Though ICOS argues, and we acknowledge, that claim 1 of the '756 patent and the specification call out other limitations with multiple components, e.g., "first camera" to take "a first image" and "second camera" to take "a second image," we do not agree that the failure to specifically refer to a "first illumination apparatus" and a "second illumination apparatus" evinces a clear intent on the part of the patentee that the term be limited to a single illumination source. Indeed, the very use of the article "an" indicates, at least presumptively, that the patentees intended the claim language "an illumination apparatus" to mean one or more illumination sources, and thus to cover implicitly "a first illumination apparatus" and subsequent "illumination apparatuses" where they exist. ***To limit the claim term "an illumination apparatus" to one illumination source, we require much stronger evidence of the patentees' intent than strained extrapolation from the language employed by the patentees in other claim limitations.*** Barring some evidence that the patentees intended to limit the claims to a single illumination source, evidence we do not find in the claim language, their use of the term "an" is consistent with multiple illumination sources.

Id. (emphasis added).

Turning to the substance of the specification, I find no evidence of a clear intent to limit "a conductor" to a "single" or "common" conductor. Figure 1 of the specification shows the following:

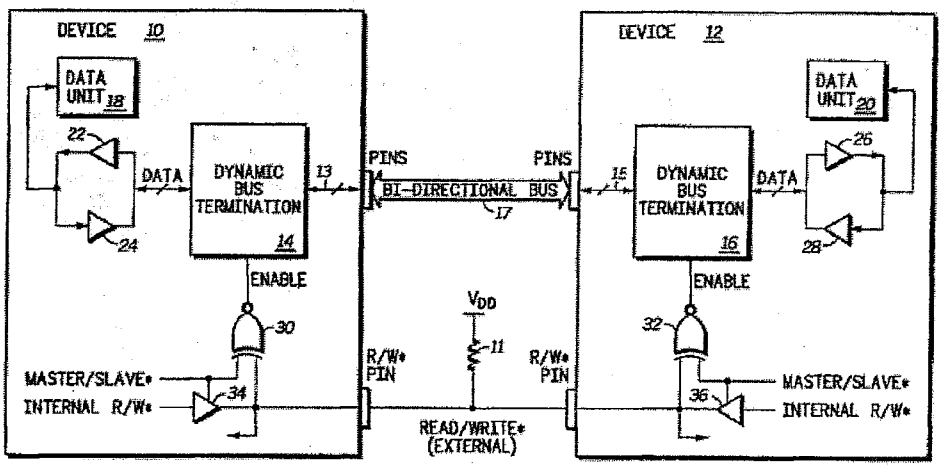

FIG. 1

(JX-1 at Fig. 1.)

The bus termination circuit 14[1] is connected to one or more external data pins via bi-directional bus 13. (JX-1 at 4:15-17.) The parties are in agreement that the slash through the bus line is an indication that the one line shown is actually multiple lines. (*See, e.g.*, Tr. at 337:6-9, 436:10-16, 438:14-20.) The bus termination circuits 14 in Figure 1 are controlled by a control signal shown as "ENABLE."[2] The specification states that "[t]he circuit component within circuit 14 is coupled to the pins in response to the state of an enable control signal of FIG. 1. The enable signal, in general, is in one logic state if a data is incoming to the device 10 and is deasserted when data is being sent out from the device 10." (JX-1 at 4:40-44.) Thus, I concur with Respondents that Figure 1 shows an embodiment where a common enable signal controls each of the bus termination circuits for each of the external pins. However, this does not serve to limit claim 9 to a common conductor. *KCJ*, 223 F.3d at 1356 ("[S]tanding alone, a disclosure of

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[1] While the specification recites bus termination circuit 14 in the singular, the parties are in agreement that item 14 represents a separate bus termination circuit for every external pin. (*See* RX-204C at Q. 204; Tr. at 243:3-244:7.) There is support for this conclusion in the specification. (*See* JX-1 at 7:44-47.)

[2] I find that the '455 patent uses the terms "control signal" and "enable signal" to refer to the same thing.

a preferred or exemplary embodiment encompassing a singular element does not disclaim a plural embodiment.")

Figure 5 depicts another embodiment of the invention and shows the following:

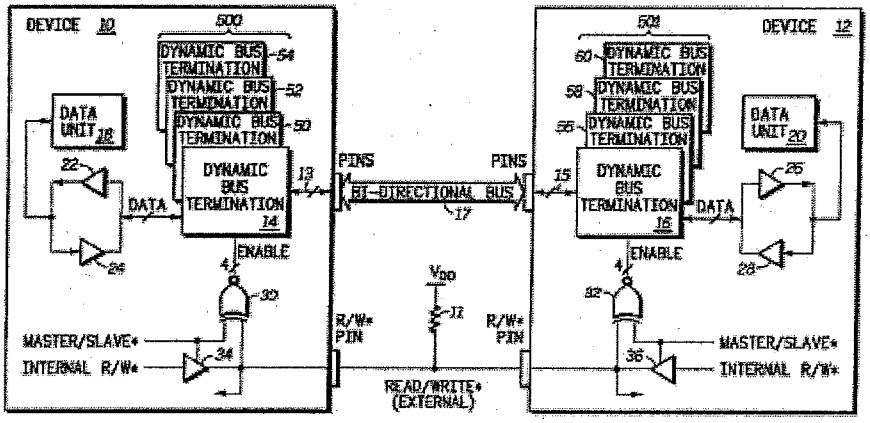

FIG. 5

(JX-1 at Fig. 5.)

Figure 5 is similar to Figure 1, but includes one major difference. Instead of a single bus termination circuit provided for each external pin, there are four bus termination circuits provided for each external pin, and four enable signals for the bus termination circuits:

> FIG. 5 illustrates a system similar to FIG. 1. All the elements of FIG. 1 which are analogous to elements in FIG. 5 are identically labeled. One significant different [*sic*] between FIG. 1 and FIG. 5 is that FIG. 5 illustrates termination circuits 500 and 501. The termination circuit 500 contains, in FIG. 5, four dynamic bus termination circuits 14, 50, 52, and 54. It should be noted that any number of bus termination circuits may be included within circuit 500. In general, N dynamic bus termination circuits may be serially connected and/or parallel-connected together in the circuit 500 wherein N is a finite integer greater than zero (i.e., 1, 2, 3, 4, 5, 6, . . . dynamic bus termination circuits may be used). Each of the bus termination circuits in circuit 500 have different enable signals, therefore four enable signals are illustrated in FIG. 5. When termination is desired, one or more of the enable signals may be enabled to connected one or more termination components/circuits to the bus to reduce signal reflection or alter line impedance.

(JX-1 at 7:9-26.)

The specification makes clear that while Figure 5 depicts only one termination circuit 500, termination circuit 500 will be repeated for each bit of the data bus 13 (*i.e.* each external pin of the device): "Note that bus 13, the bi-directional bus, and the data bus may be either one bit or more than one bit. If they are more than one bit, then circuit 500 is repeated for each bit of the bus, as in FIG. 1." (JX-1 at 7:44-47.) The specification does not state that there would be new or different enable signals for the repeated termination circuits, meaning that the four enable signals shown in Figure 5 would be common to each of the termination circuits 500 found in device 10.

Figure 6 provides a more detailed view of circuit 500 from Figure 5:

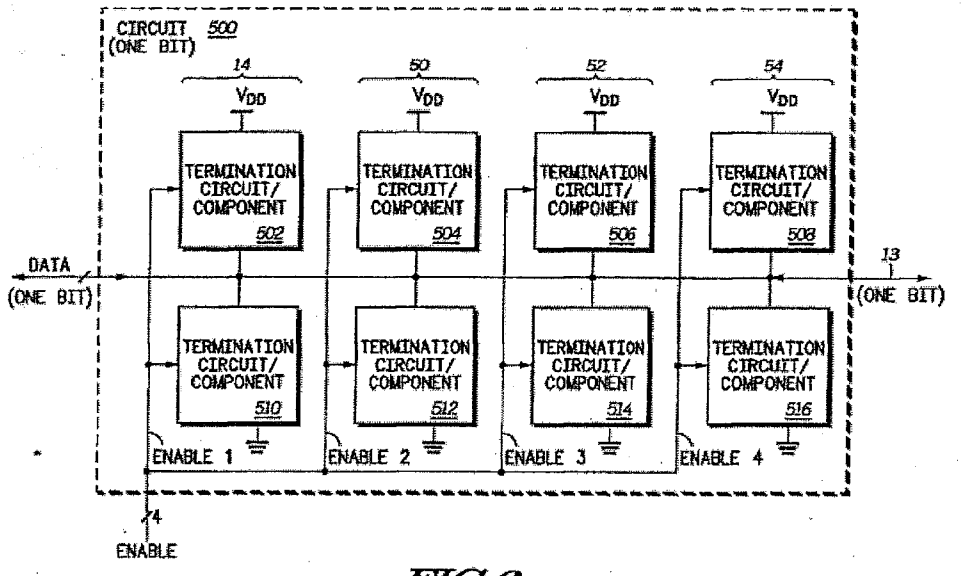

FIG.6

(JX-1 at Fig. 6.)

The specification explains:

> For example, FIG. 6 illustrates the circuit 500 including the four termination circuits 14, 50, 52, and 54. The bus 13, the data bus and four enable lines of FIG. 5 are illustrated. The 4 enable circuits are split internal to circuit 500 into separately-labeled enable signals 1 through 4.

(JX-1 at 7:48-52.)

Thus, under the embodiment shown in Figures 5 and 6, when there are, for example, two external pins and therefore two bits on the data bus 13, there will be two separate termination circuits 500, and each of these termination circuits will contain four separate bus termination circuits, 14, 50, 52, 54. (JX-1 at 7:44-47.) Yet, there will still only be four separate enable signals, meaning that there will be a common enable signal for each of the bus termination circuits 14 in the two termination circuits 500, a common enable signal for each of the bus termination circuits 50 in the two termination circuits 500, and so on.

In describing Figure 6, the specification explains that another possibility is to use two enable signals per termination circuit, with each enable signal controlling a different component found within the termination circuit: "In another form, eight enable signals may be used in FIG. 6 wherein one enable signal is coupled to each termination circuit/component of FIG. 6." (JX-1 at 8:25-28.)

In sum, I find nothing in the claim language or specification that limits "an input," "a control signal," or "a conductor" in claim 9 to the singular form. Moreover, I find that both the claim language and the specification fully supports reading "a conductor" to mean "one or more conductors."[3]

Respondents and Staff attempt to limit claim 9 to the embodiment shown in Figure 1, and I find that there is no justification for such a restrictive reading of the claim language. Respondents' and Staff's proposed constructions call for a common conductor connected to every input of every bus termination circuit. Claim 9 clearly allows for an external pin to be

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[3] The parties do not address the '455 patent prosecution history, and I find nothing in the prosecution history that is relevant and material to the parties' claim construction dispute. (*See generally* JX-2.)

connected to multiple bus terminal circuits – "each external pin is coupled to at least one bus termination circuit." Adopting Respondents' and Staff's constructions would mean that each of these bus termination circuits coupled to the external pin would be enabled or disabled via the same control signal. Such an embodiment is not contemplated, described, or depicted in the '455 patent.

The parties offer extrinsic evidence in the form of expert testimony and inventor testimony. I find it unnecessary to resort to this extrinsic evidence to determine the meaning of this claim limitation. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) ("In most situations, an analysis of the intrinsic evidence alone will resolve any ambiguity in a disputed claim term. In such circumstances, it is improper to rely on extrinsic evidence."). Assuming, *arguendo*, that I was to consider extrinsic evidence, I find that inventor testimony generally is entitled to little to no weight. *See, e.g., E-Pass Techs., Inc. v. 3Com Corp.*, 343 F.3d 1364, 1370 n. 5 (Fed. Cir. 2003) ("[T]his court has often repeated that inventor testimony is of little probative value for purposes of claim construction."); *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1379 (Fed. Cir. 2000) ("In *Markman,* we addressed the...issue of litigation-derived inventor testimony in the context of claim construction, and concluded that such testimony is entitled to little, if any, probative value.").

4. "To Decouple At Least One Circuit Component From the Bus"

The phrase "to decouple at least one circuit component from the bus" appears in asserted claim 9.

Freescale's Position: Freescale contends that "to decouple at least one circuit component from the bus" does not need to be construed, and that the plain and ordinary meaning applies.

Freescale argues that Respondents' addition of the term "previously connected" to the claim language is incorrect. Freescale asserts that the claim language itself is clear: it requires only that "at least one circuit component" be decoupled from the bus, which occurs when the claimed control signal is deasserted. (Citing JX-1 at 10:49-52; CX-401C at Q. 60-63.) Freescale claims that there is no requirement that any particular circuit component be decoupled, only that at least one circuit component is decoupled. (*Id.*)

Freescale asserts that if the claim intended to require that the decoupled circuit component(s) to be limited to the identical circuit component(s) that were coupled when the control signal is asserted, the claim would use the definite article "the" to refer back to that particular "at least one circuit component." Because the claim does not state "to decouple the at least one circuit component," Freescale argues that Respondents' position is without merit.

Freescale states that the specification does not limit the decoupled circuit component(s) to the same circuit component(s) that was previously coupled. (Citing JX-1 at 1:53-57, 4:41-50, 7:10-48, Figs. 1, 5.) According to Freescale, Respondents point exclusively to one embodiment shown in Figure 2 to support their position. (Citing RX-1C at Q. 219; MPHB at 34-35.)

Respondents' Position: Respondents contend that "to decouple at least one circuit component from the bus" means "to electrically disconnect the at least one previously connected circuit component from the bus."

Respondents assert that every embodiment of the '455 patent teaches decoupling the same circuit component from the bus that had previously been coupled to the bus. (Citing RX-1C at Q. 219.) According to Respondents, there is no reference anywhere in the '455 patent to decoupling a different circuit component from the bus than had previously been coupled to the

bus. (*Id.*) Respondents point to the Summary of the Invention of the bus termination circuit of Figure 2 as supporting their position. (Citing JX-1 at 2:2-8, 6:22-24; RX-1C at Q. 219.)

Staff's Position: Staff contends that "to decouple at least one circuit component from the bus" means "to disconnect at least one circuit component from the bus."

Staff states that every embodiment of the '455 patent discloses decoupling the same circuit component from the bus that had been previously coupled to the bus. Staff believes that Freescale's position is inconsistent with the parties' agreed-upon construction of "bus termination circuit," which requires "circuitry for signal termination that is selectively enabled or disabled in response to a control signal." Staff asserts that the specification does not disclose any technique which would indicate how one would decouple a component differently from the one previously coupled. (Citing RX-1C at Q. 219.)

Construction to be applied: "to electrically disconnect at least one previously connected circuit component from the bus."

Claim 9 requires, *inter alia*, a control signal, which "when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus" and, "when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus."

The parties dispute whether or not the "at least one circuit component" that is decoupled from the bus must be the same "at least one circuit component" that was previously coupled to the bus. Freescale asserts that the decoupled circuit component does not need to be the same circuit component that was previously coupled. Respondents and Staff believe that the claim

requires that the decoupled circuit component be a circuit component that was previously coupled to the bus.

I find that basic logic and common sense dictates that for a control signal to be able to decouple a circuit component from the bus, the circuit component had to be previously coupled to the bus. Otherwise, there can be no decoupling. To put it another way, a circuit cannot be decoupled unless it was previously coupled.

This is supported by the language of claim 9. Claim 9 explains that a circuit component is coupled to the bus when the control signal is asserted, and then, immediately after, explains that a circuit component is decoupled from the bus when the control signal is deasserted.

This is supported by the '455 patent specification. In the Summary of the Invention, one form of the "present invention" is described as follows: "The termination circuitry is enabled if the data processor is receiving data from the bus in order to reduce signal reflection on the bus. The termination circuitry is disabled if the data processor is sending data through the bus." (JX-1 at 1:53-57.) Another form of the "invention" is described as follows: "The circuitry for terminating has an input for receiving an enable signal and has one or more termination component(s). The enable signal couples the termination component to the at least one termination pin when the enable signal is asserted, and decouples the termination component from the at least one termination pin when the enable signal is deasserted." (*Id.* at 2:2-8.) The specification consistently describes an arrangement where deasserting an enable signal will decouple a previously coupled circuit component from the bus. *(See, e.g., id.* at 4:40-49, 5:62-6:29, 7:61-8:29.)

IV. INVALIDITY

A. Applicable Law

It is the respondent's burden to prove invalidity, and the burden of proof never shifts to the patentee to prove validity. *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. N.V.*, 528 F.3d 1365, 1380 (Fed. Cir. 2008). "Under the patent statutes, a patent enjoys a presumption of validity, *see* 35 U.S.C. § 282, which can be overcome only through facts supported by clear and convincing evidence[.]" *SRAM Corp. v. AD-II Eng'g, Inc.*, 465 F.3d 1351, 1357 (Fed. Cir. 2006). The clear and convincing standard was recently reaffirmed by the Supreme Court. *Microsoft Corp. v. i4i Ltd. P'ship*, 131 S.Ct. 2238 (2011) (upholding the Federal Circuit's interpretation of 35 U.S.C. § 282).

The clear and convincing evidence standard placed on the party asserting the invalidity defense requires a level of proof beyond the preponderance of the evidence. Although not susceptible to precise definition, "clear and convincing" evidence has been described as evidence which produces in the mind of the trier of fact "an abiding conviction that the truth of a factual contention is 'highly probable.'" *Price v. Symsek*, 988 F.2d 1187, 1191 (Fed. Cir. 1993) (citing *Buildex, Inc. v. Kason Indus., Inc.*, 849 F.2d 1461, 1463 (Fed.Cir.1988)).

"When no prior art other than that which was considered by the PTO examiner is relied on by the attacker, he has the added burden of overcoming the deference that is due to a qualified government agency presumed to have properly done its job[.]" *Am. Hoist & Derrick Co. v. Sowa & Sons, Inc.*, 725 F.2d 1350, 1359 (Fed. Cir. 1984). Therefore, the challenger's "burden is especially difficult when the prior art was before the PTO examiner during prosecution of the application." *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1467 (Fed.Cir.1990).

1. Anticipation

"A patent is invalid for anticipation if a single prior art reference discloses each and every limitation of the claimed invention. Moreover, a prior art reference may anticipate without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference." *Schering Corp. v. Geneva Pharm., Inc.*, 339 F.3d 1373, 1377 (Fed. Cir. 2003) (citations omitted).

2. Obviousness

Section 103 of the Patent Act states:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35 U.S.C. § 103(a) (2008).

"Obviousness is a question of law based on underlying questions of fact." *Scanner Techs. Corp. v. ICOS Vision Sys. Corp. N.V.*, 528 F.3d 1365, 1379 (Fed. Cir. 2008). The underlying factual determinations include: "(1) the scope and content of the prior art, (2) the level of ordinary skill in the art, (3) the differences between the claimed invention and the prior art, and (4) objective indicia of non-obviousness." *Id.* (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966)). These factual determinations are often referred to as the "*Graham* factors."

The critical inquiry in determining the differences between the claimed invention and the prior art is whether there is a reason to combine the prior art references. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417-418 (2007). In *KSR*, the Supreme Court rejected the Federal Circuit's rigid application of the teaching-suggestion-motivation test. The Court stated that "it can be

important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *Id.* at 418. The Court described a more flexible analysis:

> Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue...As our precedents make clear, however, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id.

Since *KSR* was decided, the Federal Circuit has announced that, where a patent challenger contends that a patent is invalid for obviousness based on a combination of prior art references, "the burden falls on the patent challenger to show by clear and convincing evidence that a person of ordinary skill in the art would have had reason to attempt to make the composition or device, . . . and would have had a reasonable expectation of success in doing so." *PharmaStem Therapeutics, Inc. v. Viacell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007).

In addition to demonstrating that a reason exists to combine prior art references, the challenger must demonstrate that the combination of prior art references discloses all of the limitations of the claims. *Hearing Components, Inc. v. Shure Inc.*, 600 F.3d 1357, 1373-1374 (Fed. Cir. 2010) (upholding finding of non-obviousness based on the fact that there was substantial evidence that the asserted combination of references failed to disclose a claim limitation); *Velander v. Garner*, 348 F.3d 1359, 1363 (Fed. Cir. 2003) (explaining that a requirement for a finding of obviousness is that "all the elements of an invention are found in a combination of prior art references").

B. Anticipation

1. Gist

Respondents' Position: Respondents contend that U.S. Patent No. 5,479,123 to Gist ("Gist") anticipates claims 9 and 10 of the '455 patent.

Respondents state that it is undisputed that Gist teaches dynamic bus termination. (Citing RX-1C at Q. 226; Tr. at 624:2-7.) Respondents claim that Freescale asserts that Gist fails to disclose only one feature of the asserted claims – a single integrated circuit that contains both a data processor and bus termination circuitry. (Citing Tr. at 624:18-625:11; CPHB at 121-130.) Respondents argue that Gist discloses an IC that contains both a data processor and bus termination circuitry. (Citing RX-6 at 5:8-12, Fig. 2; RX-1C at Q. 233-247.)

Respondents assert that there is no dispute that Gist discloses all of the other elements of claims 9 and 10. Respondents state that Gist discloses a "data processor within an integrated circuit package." (Citing RX-6 at 4:57-60, 5:8-12, Fig. 2; RX-1C at Q. 235-237; CX-401C at Q. 76.) Respondents state there is no dispute that Gist discloses "an execution unit internal to the data processor." (Citing Tr. at 621:9-11, 626:20-22; RX-6 at 1:10-16, 4:57-60, 5:8-12, Figs. 1-2; RX-1C at Q. 251.)

Respondents claim that Gist discloses "a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus." (Citing Tr. at 621:12-18, 622:13-15; RX-6 at 4:57-67, 5:19-23, Figs. 1-3; RX-1C at Q. 252-255.) Respondents state that there is no dispute that Gist discloses "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit, the plurality of bus termination circuits providing

data to or receiving data from the execution unit, each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal." (Citing Tr. at 622:13-15; RX-6 at 5:11-12, Figs. 2, 3; RX-1C at Q. 256-258, 276-277.)

Respondents state that Gist teaches "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal," as Freescale has construed "a conductor..." Respondents state that each of the bus termination circuits 47g and 48 of Gist has a conductor carrying a control signal to its respective gate terminal. (Citing RX-6 at Figs. 5A, 5B; RX-1C at Q. 281-283.)

Respondents claim that it is undisputed that Gist discloses "wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus." Respondents state that Gist discloses, for example, that when the control signal TENB is asserted high, transistor 47g is coupled to the bus to provide termination to the bus, and when TENB is low, transistor 47g is decoupled from the bus. (Citing RX-6 at 9:62-10:2, Figs. 5A, 5B; RX-1C at Q. 284-285; Tr. at 623:6-9.)

Respondents argue that Gist anticipates claim 10. Respondents claim that there can be no dispute that Gist teaches use of circuit components "selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, an electrical short circuit, and an inductor." According to Respondents, circuit components 47g and 48 of Gist are transistors. (Citing RX-6 at 9:38-41, 10:20-25; RX-1C at Q. 286.)

Freescale's Position: Freescale contends that Respondents have failed to offer clear and convincing evidence that Gist anticipates claims 9 or 10 of the '455 patent.

According to Freescale, Gist does not disclose a data processor with bus termination circuitry within the same integrated circuit. (Citing CX-408C at Q. 74-91.) Freescale argues that Respondents mistakenly contend that Gist discloses a microprocessor with integrated termination based entirely on a statement in Gist describing Figure 2. (Citing RX-6 at 5:9-12.) Freescale states that its expert testified that one of ordinary skill in the art reading Gist would understand that the disclosed termination circuitry is not part of a processor, but rather a separate, standalone ASIC physically distinct from the processor integrated circuit in the CPU module. (Citing CX-408C at Q. 84-86.)

Freescale argues that its interpretation of Gist is confirmed by a paper written by Gist. (Citing CX-381 at FSL-ITC 547554-76; CX-408C at Q. 98-105.) Freescale states that the paper is totally consistent with the disclosure of the Gist patent, namely that the bus I/O interface of the Gist patent is a separate ASIC that is part of a much larger, multiple component module, and not contained within a processor integrated circuit. (*Id.*) Freescale notes that the Administrative Law Judge in the 709 Investigation[4] agreed that Gist does not disclose the "data processor within an integrated circuit package" which also contains the "plurality of bus termination circuits" as required by claims 9 and 10. (Citing JX-55C at 76; CX-408C at Q. 92-97.)

Staff's Position: Staff contends that Gist anticipates claims 9 and 10 of the '455 patent. Staff states that Gist discloses the one element that Freescale claims is missing from the reference – the presence of a CPU on the same die with the termination circuits. (Citing RX-1C

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[4] The "709 Investigation" refers to *Certain Integrated Circuits, Chipsets, & Products Containing Same Including Televisions, Media Players, & Cameras*, Inv. No. 337-TA-709.

at Q. 233-235; RX-6 at 5:9-12.) Staff states that the evidence demonstrates that Gist expressly discloses that a CPU is part of an integrated circuit that includes the I/Os and termination circuits. (Citing Tr. at 401:15-402:10.)

Staff asserts that according to Dr. Knox, Gist specifically discloses that device 14 can be an integrated circuit 14' having a plurality of integrated bus I/O interface cells 40, which contain the dynamic bus termination disposed about the periphery of the integrated circuits. (Citing Tr. at 451:5-19.) Therefore, Staff believes that element 14' in Gist is an integrated circuit, and it contains a plurality of these dynamic bus terminations, labeled as device 50, each of which is on the same integrated circuit, and each of which connects to an external pin, which connects an external bus 30. (Citing Tr. at 451:20-452:2.)

Staff states that Gist discloses two independent termination circuits. (Citing RX-1C at Q. 281-282.) Staff notes that Gist would not anticipate if Staff's or Respondents' proposed construction of "a conductor" limitation is adopted. Staff states that because Gist discloses the use of transistors 47g and 48, the additional limitation of claim 10 is disclosed. (Citing RX-1C at Q. 286.)

Discussion and Conclusions: Based on the evidence in the record, I find that Respondents have failed to offer clear and convincing evidence that Gist anticipates claims 9 or 10 of the '455 patent.

Claim 9 requires, *inter alia*, "[a] data processor within an integrated circuit package" that contains "a plurality of bus termination circuits." The parties dispute whether or not Gist discloses this claim limitation.

Figure 1 of Gist shows the following:

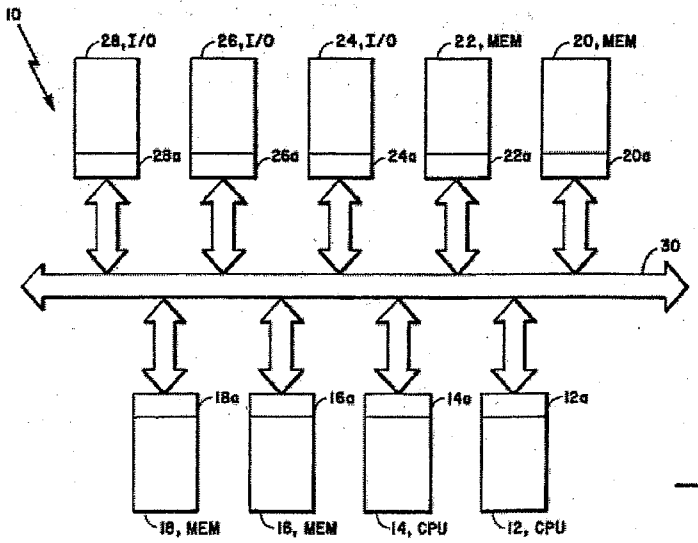

Fig. 1

(RX-6 at Fig. 1.) Gist describes Figure 1 in the following manner:

> Referring now to FIG. 1, a computer system 10 is shown to include a pair of central processing units (CPU's) 12, 14 each CPU including an interface circuit 12a, 14a respectively. The computer system 10 is shown to further include here four memory modules 16, 18, 20 and 22 each also having interface circuits 16a through 22a respectively and three I/O modules 24, 26, and 28 with each having respective interface circuits 24a, 26a and 28a, as shown. Each of the interfaces 12a through 28a are interconnected together via a system bus 30.

(RX-6 at 4:57-66.)

The parties focus on CPU 14 of Gist. Respondents contend that CPU 14 is implemented as a data processor within an integrated circuit package. (RX-1C at Q. 235.) Figure 2 of Gist shows CPU 14 in more detail:

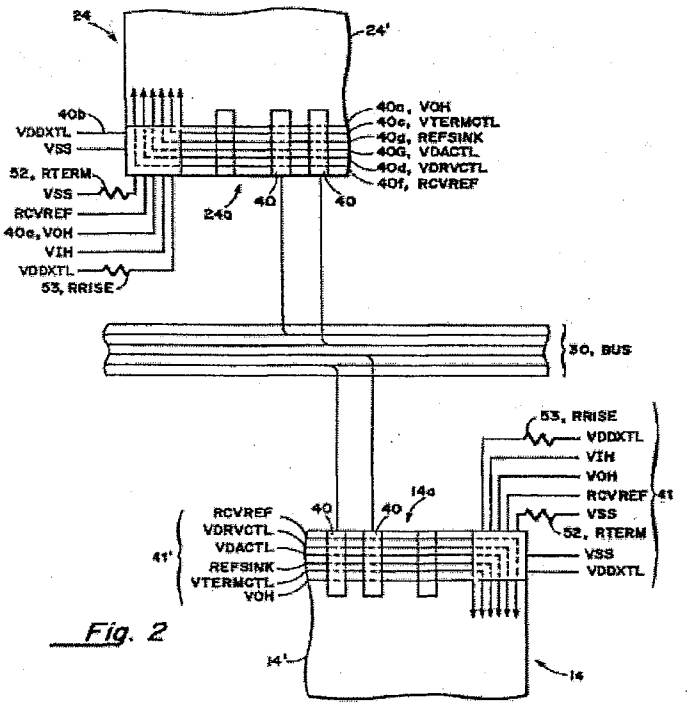

Fig. 2

(RX-6 at Fig. 2.)

The relevant portion of Figure 2 is described as follows:

Referring now to FIG. 2, a representative portion of the system 10 is shown. Here modules 14 and 24 (FIG. 1) are shown diagrammatically as integrated circuits 14' and 24' each having a plurality of integrated bus I/O interface cells 40 disposed about the periphery of the integrated circuits. Details of the interface cells 40 will be discussed in conjunction with FIGS. 3 to 20.

Suffice it to say that the devices 14 and 24, of FIG. 1 include an integrated circuit 14a' and 24a', here an ASIC (application specific integrated circuit) which is part of the interface circuit 14a and 24a to the particular device 14, 24 (FIG. 1). Each I/O cell 40 of each circuit for each device is interconnected via conductors of bus 30 which are typically disposed on a printed wiring board (PWB) such as a backplane or motherboard (not shown) to each corresponding line on the devices 12 to 28 (FIG. 1). Each of the bus interface cells are also interconnect via a interface cell control bus 41, 41' with each of said buses typically being unique for each one of said devices 12-28. Each of such buses include reference voltage signals, enable signals and supply voltage signals, as necessary for operation of integrated I/O cell circuits, as will now be described.

(RX-6 at 5:8-29.)

The parties agree that the interface circuit of Gist contains the bus termination circuits, which are part of the I/O cells 40. (RX-1C at Q. 256; CX-408C at Q. 83.) The dispute between the parties is whether these bus termination circuits are located on the same integrated circuit as the processor of CPU 14.

Dr. Knox focuses on the following sentence from Gist when rendering his opinion: "modules 14 and 24 (FIG. 1) are shown diagrammatically as integrated circuits 14' and 24' each having a plurality of integrated bus I/O interface cells 40 disposed about the periphery of the integrated circuits." (RX-6 at 5:9-12.) According to Dr. Knox, this portion of Gist "unequivocally teaches...that a single integrated circuit 14' contains the entire CPU 14 and a plurality of bus termination circuits in bus I/O interface cells 40." (RX-1C at Q. 240.)

Dr. Knox then addresses the portion of Gist that discloses placing the bus I/O interface cells on an ASIC, which is quoted above. (RX-6 at 5:15-19.) As Dr. Knox states, an ASIC is an "application specific integrated circuit." (RX-1C at Q. 244.) An ASIC "is designed and optimized for a specific application, such as communicating with a disk drive, processing video data, etc." (*Id.*) Dr. Knox acknowledges that if the bus I/O interface cells are on an ASIC, they are not necessary on the same integrated circuit as the CPU. (*Id.* at Q. 247.) But Dr. Knox claims that Gist is disclosing two different embodiments in column 5. Dr. Knox refers to the ASIC embodiment as "a possible alternative implementation of the high-level system of Figure 1." (*Id.* at Q. 245.) Dr. Knox states:

> Unlike the sentence at column 5:9-12 of Gist that teaches a single-chip implementation, the sentence at column 5:15-19 can be interpreted to allow both a single chip and a multi-chip embodiment, because it does not place any limitation on how integrated circuits 14a' and 24a' would be combined with integrated circuits 14' and 24'. For example, one could have used two separate chips, one for the CPU and one for the bus interface circuit, in order to simplify the manufacturing of the chips themselves at the expense of complicating the manufacturing of the circuit board.

(*Id.*)

Dr. Subramanian offered the opinion that Gist does not disclose alternate embodiments, as Dr. Knox claims. Dr. Subramanian states that "Gist teaches only that the termination circuit 42 is integrated in the ASIC[.]" (CX-408C at Q. 85.) Dr. Subramanian claims that "a person of ordinary skill in the art reading the Gist patent would understand that the disclosed termination circuitry is not part of the CPU, but rather a separate standalone ASIC physically distinct from the CPU in the module." (*Id.*) Dr. Subramanian opines that the portion of Gist relied upon by Dr. Knox, at column 5 lines 9 through 12, is completely consistent with the view that Gist teaches that the bus termination circuitry is located on an ASIC that is physically separate from the CPU:

> In my opinion, since there is only one embodiment in Gist of the bus interface circuits, in which they are contained within the ASIC, the sentence "[h]ere modules 14 and 24 (FIG.1) are shown diagrammatically as integrated circuits 14' and 24' each having a plurality of integrated bus I/O interface cells 40 disposed about the periphery of the integrated circuits" is completely consistent. In my opinion, that sentence does not mean that the bus interface circuits in Gist are located on the same integrated circuit die as the processor.
>
> Instead, Gist states that the bus interface circuits are "shown diagrammatically as integrated circuits" and then in the next sentence, highlighted on CDX-5.2, which is column 5, lines 15 to 19, Gist states "[s[uffice it to say that the devices 14 and 24, of FIG. 1 include an integrated circuit 14a' and 24a', here an ASIC (application specific integrated circuit) which is part of the interface circuit 14a and 24a to the particular device 14, 24 (FIG. 1)." The latter passage provides specific information about what kind of integrated circuit contains the bus interface circuits, an ASIC.

(CX-408C at Q. 86.)

From the above-described expert testimony, I find that Gist does not clearly disclose a single integrated circuit containing both the CPU and a plurality of bus termination circuits. (CX-408C at Q. 85-88.) Gist teaches inclusion of the bus termination circuitry on an ASIC, and

both experts agree that such a teaching does not preclude bus termination circuitry that is located on a different integrated circuit than the CPU. (*Id.*; RX-1C at Q. 247.)

If I were to accept Dr. Knox's view, I would have to conclude that there are two separate embodiments described at column 5 lines 8 through 29 of Gist. (RX-1C at Q. 247; CX-408C at Q. 85-88.)[5] Reading that portion of Gist, there is absolutely no indication that two separate embodiments are being disclosed. (RX-6 at 5:8-29.) I cannot find that there is clear and convincing evidence of two separate embodiments in Gist when the patent provides no indication of separate embodiments. (CX-408C at Q. 88.)

Based on the foregoing, I find that Respondents have failed to offer clear and convincing evidence that Gist anticipates claims 9 or 10 of the '455 patent.

2. Kuboki

Respondents' Position: Respondents contend that Japanese Patent Application JP H05-83113-A ("Kuboki") anticipates claims 9 and 10 of the '455 patent under Freescale's construction of the "a conductor…" claim term.

Respondents assert that Kuboki discloses a microprocessor with a dynamic, on-die bus termination circuit that is indistinguishable from that of the '455 patent. (Citing RX-1C at Q. 359, 370-374.) Respondents note that Freescale contends that Kuboki lacks two features of the asserted claims: (1) a data processor on the same die as the bus termination circuits; and (2) multiple external pins resulting in multiple bus termination circuits. (Citing CPHB at 130-134.)

Respondents assert that Figure 4 of Kuboki shows an "LSI" or "semiconductor integrated circuit device" which includes dynamic bus termination circuits as part of its I/O buffer. (Citing

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[5] To the extent that Respondents believe that Gist discloses only a single embodiment with the processor and bus termination circuitry on the same IC, I find that Respondents have not offered clear and convincing evidence of this, particularly in view of the testimony of their own expert to the contrary. (RX-1C at Q. 247.)

RX-5 at ¶ 27, Fig. 4; RX-1C at Q. 361, 363, 367-368.) Respondents state that the term "LSI" denotes an integrated circuit with a large scale of integration, such as a microprocessor. (Citing RX-1C at Q. 362.) Respondents assert that additional portions of the specification of Kuboki make perfectly clear that the data processor and bus termination circuitry can be integrated on the same IC. (Citing RX-5 at ¶¶ 1, 16, 17, 39; RX-1C at Q. 376-380.)

Respondents argue that Kuboki discloses "a plurality of external pins" and "a plurality of bus termination circuits," as required by claims 9 and 10. Respondents state that this conclusion is compelled by the disclosures of Figure 5, and specifically the use of the term "data bus" and the disclosure of an address bus with multiple lines. (Citing RX-1C at Q. 386, 388-389.)

Respondents state that Figure 5 teaches that the microprocessor connects, via conductor 35, to a "data bus line." (Citing RX-5 at Fig. 5.) Respondents claim that one of ordinary skill in the art would understand that the disclosed "data bus line" is a single data line in a data bus, a data bus contains multiple data lines, and that the disclosed microprocessor therefore has a plurality of external pins, one for each data line in the data bus. (Citing RX-1C at Q. 382-393; RX-5 at ¶¶ 16, 17, 39, Fig. 4.) Respondents state that the use of multiple address lines "A1~A7" in Figure 5 further indicates that Kuboki discloses the use of multiple data lines of a bus. (Citing RX-1C at Q. 388; Tr. at 452:11-454:24.)

Respondents note that Freescale argues that Kuboki does not inherently disclose a plurality of bus termination circuits because the bus termination circuit in Figure 4 could be used for a single serial data line. (Citing CPHB at 134; CX-408C at Q. 134.) Respondents argue that Freescale is taking an overly strict standard for inherency that requires Respondents to prove that it would be impossible to use Kuboki's circuit with a single serial line. (Citing *SmithKline Beecham Corp. v. Apotex Corp.*, 403 F.3d 1331, 1343 (Fed. Cir. 2005).)

Finally, Respondents assert that there is no dispute that Kuboki discloses the remaining elements of claim 9, and the additional element in claim 10.

Freescale's Position: Freescale contends that Respondents have failed to offer clear and convincing evidence that Kuboki anticipates claims 9 or 10 of the '455 patent.

Freescale argues that Kuboki does not disclose that the "semiconductor integrated circuit device" is incorporated into the same integrated circuit package as the microprocessor. (Citing CX-408C at Q. 122-126.) Relying on the language of Kuboki, Freescale asserts that there is no teaching that the disclosed circuitry of Kuboki is implemented within the same integrated circuit package as a microprocessor. (*Id.*)

Freescale argues that Kuboki lacks the "plurality of external pins" and "plurality of bus termination circuits" of claim 9. Freescale state that Kuboki describes termination circuitry connected to a single terminal, labeled "P1," on an integrated circuit 44, as shown in Figure 4. (Citing CX-408C at Q. 127-128.) Freescale claims that Kuboki does not disclose multiple external pins, each coupled to an input/output circuit. (Citing CX-408C at Q. 127-128, 130-137.) Freescale claims that Respondents' inherency argument is flawed. (Citing Tr. at 426:11-427:2.)

Staff's Position: Staff contends that Kuboki fails to anticipate claims 9 or 10 of the '455 patent.

Staff argues that Kuboki does not expressly disclose multiple pins, one each for each of the addresses, or a "bus" with multiple lines, either in text or in a figure. Staff states that Freescale contends that the circuit of Figure 4 could be used for a single serial data line. (Citing RX-408C at Q. 134; Tr. at 428:20-429:11.) Staff asserts that while the probability that Kuboki used a single data line is very low, "the mere possibility" that Kuboki uses a single serial data

line is sufficient to preclude a finding that Kuboki inherently discloses multiple bus termination circuits and multiple external pins.

Discussion and Conclusions: Based on the evidence in the record, I find that Respondents failed to offer clear and convincing evidence that Kuboki anticipates claims 9 or 10 of the '455 patent.

The parties dispute two claim limitations found in claims 9 and 10. First, they dispute whether or not Kuboki discloses "[a] data processor within an integrated circuit package" that contains "a plurality of bus termination circuits." Specifically, the parties dispute whether or not Kuboki teaches a single integrated circuit including both a processor and termination circuitry. I find that Kuboki clearly discloses a single integrated circuit including both a CPU and termination circuitry. Kuboki discloses nine different embodiments of termination circuitry. (*See* RX-5 at ¶¶ 7-15.) After that, it discloses a "[m]icroprocessor incorporating any one of the first through the ninth device as the input/output interface." (*Id.* at ¶ 16.) Kuboki later discloses the following:

> Although semiconductor integrated circuit devices were described in each of the aforesaid embodiments, the same effect as the aforesaid embodiments can be obtained by using these devices to constitute a microprocessor or microcomputer.

(RX-5 at ¶ 39.) The "semiconductor integrated circuit device" referenced in this passage refers to the bus termination circuitry. (*See, e.g., id.* at ¶¶ 19-27.)

Reviewing the above-quoted passages from Kuboki, Dr. Knox opined that "[t]his is unambiguous language, and since a microprocessor is itself an integrated circuit, the only logical reading of that disclosure is that Kuboki teaches a microprocessor with on-chip dynamic termination circuitry." (RX-1C at Q. 380; *see also id.* at Q. 376.) I concur, and find that the

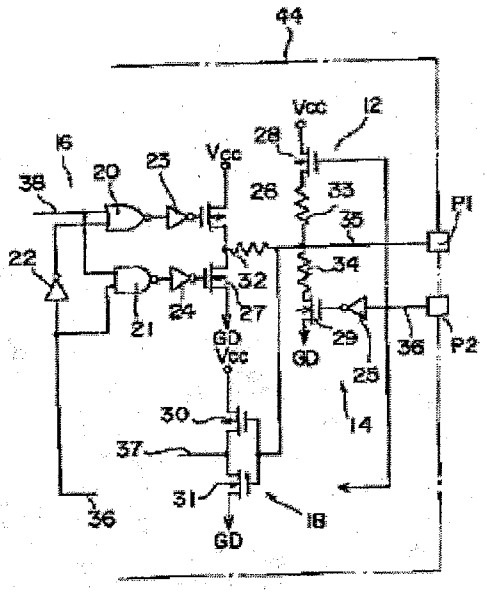
above-quoted passages from Kuboki clearly disclose a single integrated circuit including both a processor and termination circuitry.

Freescale and Dr. Subramanian focus on the microcomputer embodiments described in Kuboki and they disregard the plain language of Kuboki that states that the invention includes a "[m]icroprocessor incorporating" the bus termination circuitry. (*See, e.g.*, CX-408C at Q. 126.) As Dr. Knox opined, this unambiguous disclosure teaches a microprocessor with on-chip bus termination circuitry. (RX-1C at Q. 376, 380.)

The parties next dispute whether or not Kuboki discloses "a plurality of external pins" and "a plurality of bus termination circuits," as required by the asserted claims. I find that Respondents have failed to offer clear and convincing evidence that Kuboki discloses these claim elements.

Respondents rely on Figures 4 and 5 of Kuboki. Figure 4 shows "an embodiment of an input/output buffer with 3-station function[.]" (RX-5 at ¶ 27.)

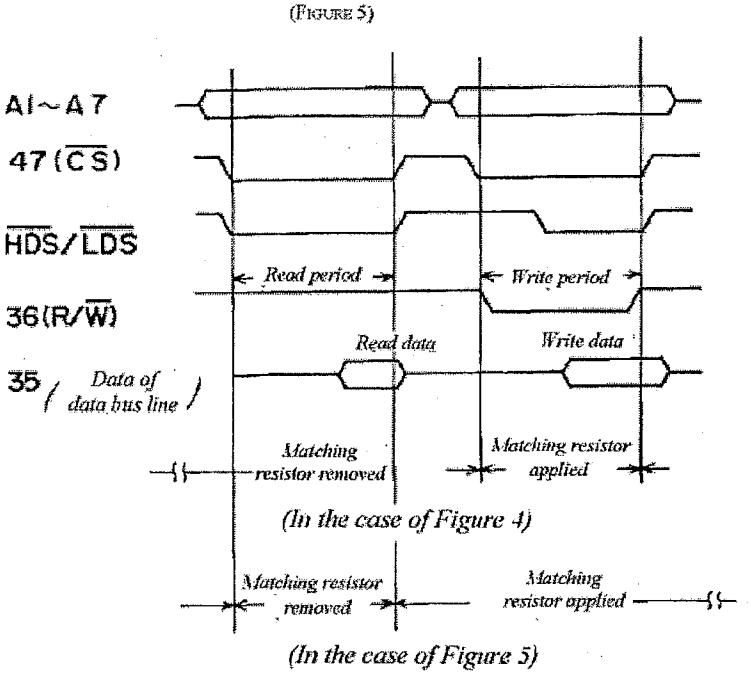
(FIGURE 4)



(RX-5 at Fig. 4.)

There is no dispute that the item labeled "P1" is an external pin, and that first clamp circuit 12 is a bus termination circuit. (RX-1C at Q. 382, 394; CX-408C at Q. 132.) The parties also agree that there is no express disclosure of multiple external pins or multiple bus termination circuits. (Tr. at 425:15-426:2, 428:3-10; CX-408C at Q. 132.) Instead, Respondents contend that Kuboki inherently discloses the use of multiple pins and multiple bus termination circuits.

Dr. Knox opines that Figure 5 of Kuboki indicates that multiple pins and multiple bus termination circuits are present. Figure 5 shows a "[t]ime chart illustrating the action of Figure 4."



(RX-5 at Fig. 5.)

Dr. Knox testified that "[e]ven though Figure 4 shows a representative circuit for pin P1, a person of ordinary skill would know that Kuboki inherently teaches applying that circuit to multiple pins on a data bus." (RX-1C at Q. 382.) To support this, Dr. Knox notes that Figure 5

refers to signal transmission route 35 as "data of data bus line." (*Id.* at Q. 386.) Dr. Knox states that "a person of ordinary skill in the art would understand Kuboki's use of the word 'bus' could only refer to multiple data lines in the context of Kuboki." (*Id.*) Dr. Subramanian agreed that a "bus" refers to multiple lines. (Tr. at 650:22-651:5.) Dr. Knox states that the notation "A1~A7" in Figure 5 indicates an address sent over multiple address lines, which is consistent with the use of multiple lines for data transmission. (*Id.* at Q. 388-389.) Dr. Knox adds that "[t]he entire disclosure of Kuboki relates to high performance microprocessors operating at high frequencies," meaning that a parallel data bus with multiple lines would be used. (*Id.* at Q. 387.)

Dr. Subramanian opines that Kuboki does not inherently disclose the use of multiple pins and multiple bus termination circuits. He states that "Kuboki never uses the word parallel, and never refers to multiple lines of a bus, and furthermore never teaches that there are multiple instances of the input/output buffer circuit." (CX-408C at Q. 132.) Dr. Subramanian offers his view that the circuit of Figure 4 could be used for a single serial data line, which would not require a plurality of external pins or bus termination circuits. (*Id.* at Q. 137.) Dr. Knox agreed that Figure 4 of Kuboki, taken out of the context of the rest of the reference, could be used for a single serial line, and not multiple parallel data lines. (Tr. at 426:11-427:2.) Dr. Subramanian opined that even though Figure 5 uses the term "bus," this is not inconsistent with his view that line 35 in Kuboki is a serial line. (Tr. at 662:16-663:10.)

A prior art reference may inherently disclose a claim limitation if the claim limitation is necessarily present in the prior art reference. *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295 (Fed. Cir. 2002) ("Inherent anticipation requires that the missing descriptive material is 'necessarily present,' not merely probably or possibly present, in the prior art.") (citation omitted); *see also Crown Packaging Tech., Inc. v. Ball Metal Beverage Container Corp.*, 635

F.3d 1373, (Fed. Cir. 2011) (explaining that "inherent anticipation requires more than mere probabilistic inherency[.]") A district court summed up the law of inherency by explaining:

> To establish inherency, the anticipatory feature or result must be consistent, necessary, and inevitable, not simply possible or probable, and it should be clear that it would be so recognized by persons of ordinary skill. That is, inherency may not be established by probabilities or possibilities, and the mere fact that a certain thing may result from a given set of circumstances is not sufficient to show inherency.

Allergan, Inc. v. Sandoz Inc., 818 F. Supp. 2d 974, 1003 (E.D. Tex. 2011) (citations omitted).

Here, Respondents' inherency argument is based on two disclosures in Figure 5 of Kuboki that are not explained in Kuboki's specification – the "A1~A7" reference, and the reference to a "bus." Respondents, through Dr. Knox, contend that those references make clear that the external pin and bus termination circuit of Figure 4 will be repeated multiple times, resulting in a plurality of external pins and a plurality of bus termination circuits. (RX-1C at Q. 382-389, 397-398.) While these two references in Figure 5 make it possible, even probable, that there are multiple external pins and bus termination circuits, I cannot find that these elements are ***necessarily*** present.

First, Dr. Subramanian offers an opinion regarding a plausible configuration of Kuboki that would not require multiple external pins and multiple bus termination circuits. (CX-408C at Q. 137; Tr. at 662:16-663:10.) Second, Kuboki does not contain any explanation of the references in Figure 5. To find that the limitations are inherently disclosed requires that I make a number of logical leaps based solely on Dr. Knox's challenged testimony, namely that (1) the "A1~A7" and "bus" references necessarily mean that there are multiple signal transmission routes similar to signal transmission route 35; (2) that each of these multiple signal transmission routes is connected to an its own external pin similar to P1; and (3) that each of these multiple signal transmission routes is connected to its own bus termination circuitry similar to first clamp

circuit 12. (RX-1C at Q. 382-389, 397-398.) I find that there is insufficient evidence in the record to make these logical leaps and conclude that the evidence clearly demonstrates that Kuboki inherently discloses the multiple external pins and multiple bus termination circuit references.

C. Obviousness

1. Gist In Combination With The Knowledge of One Of Ordinary Skill In The Art and/or Kuboki

Respondents' Position: Respondents contend that if Gist is not found to anticipate claims 9 and 10 of the '455 patent, the combination of Gist with the knowledge of one of ordinary skill in the art, or the combination of Gist and Kuboki both render those claims obvious.

Respondents note that the only limitation that Freescale argues is missing from Gist is a data processor and bus termination circuitry on the same IC package. Respondents argue that it would have been obvious to one of ordinary skill in the art to include the processor in the same IC package as the bus termination circuitry. (Citing RX-1C at Q. 303-305, 306-322.) Respondents claim that at the time of the filing of the '455 patent, there was a long-standing, industry-wide trend toward integrating more and more functionality and circuitry onto a single chip – a trend driven by the desire to minimize, integrate, and make semiconductor circuits more efficient and reliable. (Citing RX-1C at Q. 29, 138-139, 144-150, 435; RX-31 at 52.) Respondents note that Dr. Subramanian admitted that in 1993 there was a general trend in the industry toward increasing integration. (Citing Tr. at 656:2-7.)

Respondents claim that microprocessors with on-chip bus termination circuits were already known in the art. (Citing Tr. at 617:4-8.) Respondents assert that since the concept of integrating a microprocessor with bus termination circuitry was already known, a person of

ordinary skill in the art would have considered it obvious to integrate the CPU and the dynamic termination circuitry of Gist.

Respondents claim that the fact that a data processor with termination circuitry on the same semiconductor die did not exist in the market prior to the '455 patent is not a reason to find that the '455 patent is not obvious. As an example, Respondents note that when the '455 patent was filed, Motorola employed the named inventors. (Citing Tr. at 629:21-24.) Yet, Respondents state that Motorola did not offer any commercial product that embodied the '455 patent until approximately ten years after the filing of the Gist patent. (Citing JX-15C at 75:15-76:8; Tr. at 630:14-19.) Respondents state that the reason for the delay related to cost and marketability, and not technical hurdles. (Citing JX-15C at 61:1-16.) Respondents contend that in the 1993 time frame, a product with the processor and the bus termination circuitry was possible, but it would have required a relatively expensive cooling apparatus on the device. (Citing RX-1C at Q. 319-320.)

Respondents argue that if the "a conductor..." claim limitation is construed to require a common conductor, it would have been obvious to modify Gist to utilize a common conductor. Respondents assert that the use of a common conductor to carry the control signal would have been an obvious design choice in view of the knowledge of a person of ordinary skill in the art. (Citing RX-1C at Q. 343-344, 345-354.)

Respondents assert that Gist and Kuboki both relate to the use of bus termination circuitry to solve the same problem. (Citing RX-1C at Q. 464.) Respondents state that there is an express motivation to combine the references found in U.S. Patent No. 5,162,672 ("McMahan"). (Citing RX-18; RX-1C at Q. 465.) Respondents assert that the combined

teachings of Gist and Kuboki would lead to a predictable result that would successfully result in the invention disclosed in claims 9 and 10. (Citing RX-1C at Q. 455, 469, 470.)

Freescale's Position: Freescale contends that Gist does not render claims 9 and 10 of the '455 patent obvious.

Freescale argues that Respondents' obviousness position is a hindsight-based conclusion that is undercut by Respondents' failure to identify even a single data processor with termination circuitry on the same semiconductor die before the '455 patent was filed. (Citing CX-408C at Q. 110-113; Tr. at 387:11-19.) Freescale claims that Respondents failed to explain why a person of ordinary skill in the art would have replaced the termination circuitry of one reference with that of another, as each circuit has its own construction, attributes, and signals. (Citing CX-408C at Q. 116-117.)

Freescale argues that it was not merely cost and marketability that precluded processors implementing the invention of the '45 patent for years after the filing of the '455 patent. Freescale states that one of the inventors testified that there were technical reasons why Motorola could not implement the '455 patent invention in the MC68000 processor line. (Citing JX-15C at 75:15-77:1.) Freescale claims that even if the only problems related to cost and marketability, that fact alone weighs against a finding of obviousness because a person of ordinary skill in the art would not be motivated to pursue the integrated approach due to the non-technical hurdles.

Staff's Position: Staff contends that to the extent that Gist is not found to anticipate the asserted claims, it renders the claims obvious. Staff states that Gist provides the suggestion of integrating each of the components with their termination circuits by describing them as being an integrated circuit. (Citing RX-6 at 5:8-12.) To the extent that this passage is not found to

disclose an integrated processor and bus termination circuit, Staff argues that it provides a suggestion to integrate.

Discussion and Conclusions: Based on the evidence in the record, I find that Respondents have offered clear and convincing evidence that Gist in combination with the knowledge of one of ordinary skill in the art and/or Kuboki renders claims 9 and 10 of the '455 patent obvious.

As described in more detail in Section IV.B.1 *supra*, the parties only dispute whether or not Gist is missing a single limitation from claim 9 – a processor and dynamic bus termination circuitry on a single chip. With regard to the remaining claim limitations from claim 9, I find that the undisputed evidence from Respondents clearly demonstrates that these limitations are disclosed in Gist. (*See* RX-1C at Q. 235-237, 251-285.)

In Section IV.B.1 *supra*, I found that Gist failed to clearly disclose a processor and bus termination circuitry on a single chip. Dr. Subramanian testified that Gist instead discloses that the bus termination circuitry is located on an ASIC that is physically separate from the processor. (CX-408C at Q. 85.) Respondents and Staff contend that, if this view is accepted, it would have been obvious to one of ordinary skill in the art to integrate the processor and the bus termination circuitry on a single chip.

I find that Dr. Knox offered credible testimony that one of ordinary skill in the art at the time of the filing of the '455 patent would have found it obvious to integrate the processor and the bus termination circuitry of Gist on a single chip. Dr. Knox testified that "[t]he motivation and trend to integrate features onto single integrated circuits, which had begun long before 1993, was a matter of routine design and manufacturing economics…This type of integration was certainly not something that a person of ordinary skill could not do, or would be discouraged

from doing." (RX-1C at Q. 306.) Dr. Subramanian agreed that in 1993, there was a general trend in the industry towards increasing integration on integrated circuits. (Tr. at 656:2-7.) Dr. Knox added that "[i]t would have been a routine exercise to take the two chips' designs and lay them out on a single integrated circuit that performs the functions of the two individual chips." (RX-1C at Q. 309.)

Dr. Knox explained that one of ordinary skill in the art would have been motivated to integrate the processor and the bus termination circuitry on a single chip to achieve benefits related to reduced size, reduced costs, reduced power consumption, and increased speed. (RX-1C at Q. 312-314.) Dr. Knox opined that one of ordinary skill in the art would have had a reasonable expectation of success in integrating the processor and bus termination circuitry of Gist on a single chip, as "integration of multiple functionalities into a single integrated circuit was routinely practiced in the industry." (*Id.* at Q. 315; *see also id.* at Q. 310.)

Dr. Knox cites to an April 1992 IEEE article, published prior to the filing of the '455 patent, as support for the proposition that one of ordinary skill in the art would be motivated to integrate the processor and bus termination circuitry of Gist onto a single chip. (RX-1C at Q. 149.) The article, entitled "ICs: the brains of a workstation" includes the following statement:

> In all devices, the trend is to higher levels of system integration, with more functions or capacity on each chip. This trend reduces system cost and increases system reliability. Equally important, it also increases speed because on-chip connections are shorter and many interchip connections are eliminated.

(RX-31 at 52.) The article further states that "examples of highly integrated microprocessors abound." (*Id.* at 53.) This article clearly supports Dr. Knox's opinion that one of ordinary skill in the art at the time of filing would be highly motivated to alter the teachings of Gist to integrate the processor and the bus termination circuitry on a single chip.

Finally, I have already found that there is prior art teaching the integration of a processor and bus termination circuitry on a single chip. In Section IV.B.2 *supra*, I concluded that Kuboki includes an unambiguous disclosure of a microprocessor with on-chip dynamic bus termination circuitry. (RX-5; RX-1C at Q. 376, 380.) Both Kuboki and Gist are related to the same subject matter, namely dynamic bus termination circuitry. (*See* RX-5; RX-6.) Thus, it would be natural for one of ordinary skill in the art to look to the teachings of Kuboki to modify the structure of Gist to integrate the processor and bus termination circuitry. (RX-1C at Q. 457.)

In sum, I find that there is clear evidence that the step of integrating the processor and the bus termination circuitry of Gist onto a single chip would have been an obvious step that one of ordinary skill in the art would know to take. Moreover, I find that one of ordinary skill in the art would have a reasonable expectation of success in performing such integration. Finally, I find that the evidence clearly supports a conclusion that there would be a motivation to perform such an integration, as doing so would lead to reduced size, reduced costs, reduced power consumption, and increased speed.

Freescale argues that the claims are not obvious; but I find that Freescale's arguments lack merit. Freescale asserts that if it was obvious to integrate the processor and bus termination circuitry, there would have been at least one example of such integration in the prior art. (CX-408C at Q. 113.)

Citing to the testimony of Mr. Gay, Freescale argues that there were reasons why one of ordinary skill in the art would not have integrated the processor and bus termination circuitry at the time of the '455 patent. Mr. Gay testified regarding why Motorola did not incorporate the invention of the '455 patent into its next microprocessor design after the inventors had conceived of the invention. (JX-15C at 60:11-19.) Specifically, Mr. Gay testified that at the time,

integrating the bus circuitry and processor onto a single chip would have required more power to the chip, which would have increased the heat to the chip. (*Id.* at 61:1-12.) Mr. Gay stated that this would have required a more expensive method to dissipate the heat. (*Id.* at 61:1-16.) Dr. Knox acknowledged this issue as well. (RX-1C at Q. 320.)

I find that Freescale's arguments miss the mark. In Section IV.B.2 *supra* I found that Kuboki discloses an integrated processor and bus termination circuitry. The technical and/or financial problems faced by Mr. Gay and Motorola in incorporating the claimed invention into a commercial product do not negate the fact that a prior art reference expressly discloses incorporating bus termination circuitry on a microprocessor.

While Dr. Subramanian testified in his witness statement that combining the processor and the bus termination circuitry on the same integrated circuit die was not known in the prior art (CX-408C at Q. 113), his testimony on cross examination tells otherwise. In two separate instances, Dr. Subramanian admitted during cross examination that putting a processor and bus termination circuitry on the same integrated circuit die was known in the prior art:

> Q. Now, you testified on Wednesday that you believe the novel aspect of the '455 patent is the idea of combining three features, a data processor, ***on-die termination***, and dynamic termination, correct?
> A. Yes, that's true.
> Q. And you also agreed with me that each of those features existed in the prior art, correct?
> A. Individually, yes.

(Tr. at 614:16-25) (emphasis added).

> Q. Let me just make sure I have a clean question. Microprocessors with on-chip bus termination circuits were also known before the '455 patent, correct?
> A. Yes.

(*Id.* at 617:4-8.)

Freescale attempts to brush aside this testimony by claiming that "[i]t is clear that Dr. Subramanian misspoke" when admitting that microprocessors with on-chip bus termination circuits were known prior to the '455 patent. (CRB at 37, n. 5.) The evidence does not support a finding that Dr. Subramanian merely misspoke when providing this testimony. First, Dr. Subramanian made this admission twice, in separate questions from counsel. Second, the questions from counsel were in no way vague or ambiguous, nor were Dr. Subramanian's responses. Third, Freescale did not attempt to resolve these alleged mis-statements through re-direct. (Tr. at 663:11-12.) I find that this testimony on cross examination supports Respondents' assertion that it would have been obvious to integrate the processor and bus termination circuitry of Gist on a single semiconductor die. *Davis v. Alaska*, 415 U.S. 308, 315 (1974) ("Cross-examination is the principal means by which the believability of a witness and the truth of his testimony are tested."); *California v. Green*, 399 U.S. 149, 158 (1970) (stating that cross examination is "the 'greatest legal engine ever invented for the discovery of truth'") (citation omitted).

Claim 10 depends from claim 9 and adds the requirement that "the at least one circuit component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, an electrical short circuit, and an inductor." Claim 10 is written as a Markush group. *Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1372 (Fed. Cir. 2005) ("A Markush group lists specified alternatives in a patent claim, typically in the form: a member selected from the group consisting of A, B, and C.") The Federal Circuit has held that a Markush group limitation is disclosed in the prior art if one of the alternatives is found in the prior art. *Fresenius USA, Inc. v. Baxter Int'l, Inc.*, 582 F.3d 1288, 1298 (Fed. Cir. 2009) ("Element (a) is written in Markush form, such that the entire element is

disclosed by the prior art if one alternative in the Markush group is in the prior art.") Dr. Knox opines that Gist discloses use of a transistor as "the at least one circuit component," and Freescale does not dispute that opinion. (RX-1C at Q. 286.) Therefore, I find clear and convincing evidence that claim 10 is obvious.

Based on the foregoing, I conclude that Respondents have offered clear and convincing evidence that claims 9 and 10 of the '455 patent are obvious in view of Gist combined with the knowledge of one of ordinary skill in the art and/or Kuboki.

2. Kuboki In Combination With The Knowledge of One Of Ordinary Skill In The Art and/or Gist

Respondents' Position: Respondents contend that if Kuboki is not found to anticipate claims 9 and 10 of the '455 patent, the combination of Kuboki with the knowledge of one of ordinary skill in the art, or the combination of Kuboki and Gist both render those claims obvious.

Respondents claim that to the extent that Kuboki is determined not to disclose a processor and termination circuitry integrated onto one integrated circuit, it would have been obvious to one of ordinary skill in the art that the processor and termination circuitry of Kuboki could be integrated. (Citing RX-1C at Q. 421-423, 424-435.) Respondents state that this is so for the same reasons already described in Section IV.C.1 *supra*.

Respondents claim that to the extent that Kuboki is found to only disclose a single termination circuit for a single pin, it would have been obvious to one of ordinary skill in the art to implement the teachings of Kuboki in microprocessor technology using a parallel data bus and, thus, including multiple pins and multiple bus termination circuits. (Citing RX-1C at Q. 408-409, 410-420.) Respondents assert that Gist discloses a parallel bus, and that it would have been obvious to combine Kuboki and Gist to use the bus termination circuitry of Kuboki with the parallel bus of Gist. (Citing RX-1C at Q. 452-470.)

Respondents state that a parallel data bus with multiple lines was a standard feature for high performance microprocessors in 1993, before the filing of the '455 patent. (Citing RX-1C at Q. 410.) According to Respondents, it would have been a matter of routine design choice to replicate the device shown in Figure 4 of Kuboki for each of the plurality of external pins that couple to the parallel data bus. (Citing RX-1C at Q. 413.) Respondents claim that there would have been no obstacles to using the technology of Kuboki on a parallel data bus. (Citing RX-1C at Q. 415-416.) Respondents claim that there would have been a motivation to use the technology of Kuboki with a parallel data bus. (Citing RX-1C at Q. 417-420.)

Respondents argue that if the "a conductor..." claim limitation is construed to require a common conductor, it would have been obvious to modify Kuboki to utilize a common conductor. Respondents assert that the use of a common conductor to carry the control signal would have been an obvious design choice in view of the knowledge of a person of ordinary skill in the art. (Citing RX-1C at Q. 471-472, 473-482.)

Freescale's Position: Freescale contends that claims 9 and 10 are not obvious in view of combinations involving Kuboki.

Freescale offers the same argument it offered with respect to Gist regarding why it would not be obvious to one of ordinary skill in the art to incorporate termination circuitry on the same semiconductor die as a microprocessor in 1993. (Citing CX-408C at Q. 146-149, 152-153.) Freescale argues that combination of Kuboki and Gist does not render the claims obvious because it lacks "a data processor within an integrated circuit package" that contains the required "plurality of bus termination circuits" that are in turn coupled to a "plurality of external pins." (Citing CX-408C at Q. 156-157.) Moreover, Freescale claims that Respondents fail to explain why a person of ordinary skill in the art would have discarded the termination circuitry of one of

these references and replaced it with the very different and incompatible termination circuitry of the other reference. (*Id.*)

Staff's Position: Staff contends that Kuboki, along with the knowledge of one of ordinary skill in the art, renders claims 9 and 10 obvious.

Staff states that it would have been obvious to one of ordinary skill in the art to add the multiple external pins and a parallel bus to Kuboki. Staff states that if its construction of "a conductor..." is adopted, it would have been obvious to use a single conductor because the evidence demonstrates that using a single conductor versus multiple conductors is a design choice. (Citing Tr. at 435:15-18.)

Discussion and Conclusions: Based on the evidence in the record, I find that Respondents have offered clear and convincing evidence that Kuboki in combination with the knowledge of one of ordinary skill in the art and/or Gist renders claims 9 and 10 of the '455 patent obvious.

In Section IV.B.2 *supra*, I addressed Respondents' contention that Kuboki anticipates claims 9 and 10. I addressed two limitations of claim 9, and found that Kuboki clearly discloses "[a] data processor within an integrated circuit package" with integrated bus termination circuitry. I did not find that Kuboki anticipates claims 9 and 10 because I found that it did not clearly disclose "a plurality of external pins" and "a plurality of bus termination circuits." Respondents offered undisputed evidence that Kuboki teaches all of the remaining elements of claim 9. (RX-1C at Q. 376-378, 381, 395-396, 399-405.)

Respondents allege that it would have been obvious to one of ordinary skill in the art to use the dynamic bus termination circuitry of Kuboki with a parallel bus, thereby resulting in a plurality of external pins and a plurality of bus termination circuits. As Dr. Knox opined:

> Under the assumption that Kuboki only discloses dynamic on-die termination for a single data line, a person of ordinary skill would have found it obvious to modify the teachings of Kuboki to include a data bus with multiple lines. A parallel data bus with multiple lines was a standard feature for high performance microprocessors in 1993, and Kuboki's microprocessor is certainly a high performance microprocessor since it operates at frequencies high enough to cause transmission line effects.

(RX-1C at Q. 410.) Dr. Knox testified that use of a parallel data bus with multiple lines would require the use of a plurality of external pins, one pin for each data line. (*Id.* at Q. 412.) Dr. Knox testified that it would have been a matter of routine design choice to replicate the bus termination circuitry shown in Figure 4 for each data line, thereby resulting in a plurality of bus termination circuits. (*Id.* at Q. 413.) Dr. Knox stated that Gist teaches the use of bus termination circuitry in the context of a parallel data bus. (*Id.* at Q. 453-454, 459-460

Dr. Knox opined that there would not have been any obstacles associated with using Kuboki's bus termination circuitry in a parallel bus structure, "because bus I/O interfaces are modular, and are generally obtained by replicating a bus I/O cell for a single data line." (RX-1C at Q. 416.) Dr. Knox stated that one of ordinary skill in the art would have been motivated to make this modification of Kuboki because use of a parallel bus with multiple data lines increases the data transmission rate of the bus. (*Id.* at Q. 417-418.)

Dr. Subramanian does not offer much in the way of a response to Dr. Knox's above-described opinions. He stated the following:

> As I testified previously, it is my opinion was that [*sic*] Kuboki does not explicitly or inherently disclose a parallel data bus, and therefore that Kuboki did not meet several limitations of claims 9 and 10, such as "a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus" and a "plurality of bus termination circuits." Even if it were obvious to use multiple instances of the input/output buffer of Kuboki when applied to a parallel bus, the results "semiconductor integrated circuit device" is still not integrated into a "data processor within an integrated circuit package,"

> which does not meet all the elements of claims 9 and 10 of the '455 patent, and therefore does not render those claims obvious, in my opinion.

(CX-408C at Q. 151.) The above-quoted testimony does not offer any rebuttal to Dr. Knox's position that it would have been obvious to modify Kuboki for use with a parallel bus. Instead, Dr. Subramanian reiterates his views that Kuboki doesn't disclose a parallel bus and that Kuboki does not disclose a processor and bus termination circuitry on the same chip. (*Id.*) Thus, I find that Dr. Knox's testimony at RX-1C, Questions 408-420 regarding the modification of Kuboki for use with a parallel data bus is unrebutted.

Claim 10 depends from claim 9 and adds the requirement that "the at least one circuit component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, an electrical short circuit, and an inductor." Dr. Knox opines that Kuboki discloses use of a resistor as "the at least one circuit component," and Freescale does not dispute that opinion. (RX-1C at Q. 406.) Therefore, I find clear and convincing evidence that claim 10 is obvious.

Based on Dr. Knox's unrebutted testimony, I conclude that Respondents have offered clear and convincing evidence that Kuboki in combination with the knowledge of one of ordinary skill in the art and/or Gist renders claims 9 and 10 of the '455 patent obvious.

3. Secondary Considerations

Freescale's Position: Freescale contends that there are several secondary considerations of non-obviousness that would weigh against a finding of obviousness.

Freescale claims that the commercial impact of the technology claimed in the '455 patent has been substantial. (Citing CX-408C at Q. 166-168.) Freescale asserts that MediaTek and Zoran ICs practice the asserted claims of the '455 patent in several families of ICs, which are then used in several categories of high-volume consumer electronics.

Freescale asserts that the '455 patent has been widely licensed within the industry. (Citing CX-408C at Q. 166-168.) Freescale argues that the licensing activity is driven by the fact that the '455 patent invention reduces signal reflection on the buses without consuming more power than needed. (*Id.*)

Respondents' Position: Respondents contend that there is no evidence of secondary considerations. Respondents claim that the '455 patent is not a "pioneer" patent, has not gained recognition in the industry, and did not solve a problem where others had failed. (Citing SPHB at 36-37; JX-16C at 83:17-22, 192:7-25; RX-1C at Q. 569-571.)

Respondents state that Freescale's argument that the technology of the '455 patent has had a substantial commercial impact fails because MediaTek and Zoran do not infringe the '455 patent. Moreover, Respondents claim that there is no evidence of nexus between the claimed invention of the '455 patent and the commercial success of Respondents' products.

Respondents argue that Freescale's position that the widespread licensing of the '455 patent supports a finding of non-obviousness fails because Freescale has not established a nexus between the licensing and the claimed invention of the '455 patent. Respondents state that the '455 patent is licensed as part of a large portfolio consisting of over 6,200 patent families. (Citing CX-402C at Q. 11, 31, 42, 45; JX-16C at 22:15-17, 27:11-20, 59:7-15, 77:19-23, 84:4-7, 88:14-89:2, 228:7-15; RX-1C at Q. 569-571.) Respondents assert that Freescale has not shown that any licensee actually practices the '455 patent, much less the asserted claims. (Citing RX-1C at Q. 572-573.) According to Respondents, Freescale has not demonstrated that the licensees entered into the licenses for any reason other than to avoid costly litigation or for business reasons unrelated to the claimed invention of the '455 patent.

Staff's Position: Staff contends that there is no evidence of secondary considerations in the record.

Staff asserts that the '455 patent is not a "pioneer" patent and has not gained recognition in the industry. Staff claims that there is no evidence that any entity has ever practiced the '455 patent in the United States. Staff states that the '455 patent has always been licensed as part of a larger portfolio, and there is no evidence that any licensee has ever actively sought a license from Freescale. Instead, Staff claims that the only evidence is that Freescale has approached entities with threats of lawsuits if they do not take a license.

Discussion and Conclusions: Based on the evidence in the record, I find no evidence of secondary considerations that would overcome the showing of obviousness addressed in Sections IV.C.1-2 *supra*.

Secondary considerations may include evidence of copying, long felt but unsolved need, failure of others, commercial success, unexpected results created by the claimed invention, unexpected properties of the claimed invention, licenses showing industry respect for the invention, and skepticism of skilled artisans before the invention. *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998). Reviewing the evidence of secondary considerations is an important step in the obviousness analysis. As explained by the Federal Circuit:

> It is jurisprudentially inappropriate to disregard any relevant evidence on any issue in any case, patent cases included. Thus evidence rising out of the so-called "secondary considerations" must always when present be considered en route to a determination of obviousness. Indeed, evidence of secondary considerations may often be the most probative and cogent evidence in the record. It may often establish that an invention appearing to have been obvious in light of the prior art was not. It is to be considered as part of all the evidence, not just when the decisionmaker remains in doubt after reviewing the art.

Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 1538-39 (Fed. Cir. 1983) (citations omitted).

Even when evidence of secondary considerations is present, it cannot overcome a strong *prima facie* showing of obviousness. *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1246 (Fed. Cir. 2010); *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007).

Freescale offers two arguments regarding secondary considerations. First, Freescale claims that "the commercial impact of the technology claimed in the '455 patent has been substantial" due to Respondents' alleged infringement of the '455 patent. In other words, Freescale claims that there is evidence of commercial success due to Respondents' infringement of the '455 patent. *See Brown & Williamson Tobacco Corp. v. Philip Morris Inc.*, 299 F.3d 1120, 1130 (Fed. Cir. 2000) ("Our case law provides that the success of an infringing product is considered to be evidence of the commercial success of the claimed invention.")

Regardless of whether or not Respondents infringe the '455 patent (an issue addressed in detail in Section VI, *infra*), Freescale offers no evidence of the commercial success of Respondents' products. (CIB at 63.) Freescale only cites to Dr. Subramanian's testimony, which contains no reference to Respondents' alleged commercial success. (CX-408C at Q. 166-168.) Therefore, I find that Freescale's commercial success argument necessarily fails, independent of the infringement determination.

Second, Freescale claims that its licensing activities constitute evidence of the non-obviousness of the '455 patent. Specifically, Freescale claims that the '455 patent has been "widely licensed within the industry." (CIB at 63.) Freescale cites to Dr. Subramanian's testimony that Freescale has licensed its patent portfolio seven times. (CX-408C at Q. 168.) Dr. Subramanian states that these licenses are compelling evidence that companies that manufacture products that incorporate the inventions of claims 9 and 10 of the '455 patent, such as Panasonic Corporation, place a high value on the '455 patent. (*Id.*)

In explaining the relevance of licensing as a secondary consideration, the Federal Circuit has cautioned that:

> Such [licensing] programs are not infallible guides to patentability. They sometimes succeed because they are mutually beneficial to the licensed group or because of business judgments that it is cheaper to take licenses than to defend infringement suits, or for other reasons unrelated to the unobviousness of the licensed subject matter. Such a "secondary consideration" must be carefully appraised as to its evidentiary value and we have tried to do that here.

EWP Corp. v. Reliance Universal Inc., 755 F.2d 898, 907-908 (Fed. Cir. 1985). The Federal Circuit also explained that "[l]icenses taken under the patent in suit may constitute evidence of nonobviousness; however, only little weight can be attributed to such evidence if the patentee does not demonstrate 'a nexus between the merits of the invention and the licenses of record.'" *In re GPAC Inc.*, 57 F.3d 1573, 1580 (Fed. Cir. 1995) (citation omitted).

I find that Freescale has offered no evidence of a nexus between the merits of the invention and the licenses. Freescale cites to Dr. Subramanian's unsupported testimony regarding the importance of the licenses to Freescale's licensees. (CX-408C at Q. 168.) Dr. Subramanian points to no evidence of the "high value" that the licensees place on the '455 patent. (*Id.*) Furthermore, Dr. Subramanian cannot substantiate his claim that any of the licensees actually practice the '455 patent. (*Id.*) Such conclusory testimony is insufficient to demonstrate a nexus between Freescale's licenses and the merits of the invention.

Based on the foregoing, I find no evidence of secondary considerations that would overcome the showing of obviousness made by Respondents.

V. ISSUE PRECLUSION

Zoran's Position: Zoran contends that Freescale's claims against Zoran are precluded in part by the doctrine of issue preclusion.

Zoran argues that Freescale cannot re-litigate the issue of whether the same Zoran products infringe the same asserted claims of the same patent that were found not infringed in the 709 Investigation. Zoran asserts that the following eight Zoran products were already adjudicated in the 709 Investigation: ZR39770BGCF; ZR39772HGCF-B; ZR39775HGCF-B; ZR39775HGCF-TC; ZR39775HGCF-TC-LP; ZR39785HGCF-B; ZR39787HGCF; and ZR39787HGCF-LP. Zoran argues that the remaining products accused of infringement in this investigation are essentially the same as the previously adjudicated products because all of the products use the same resistor-based termination circuits. (Citing RX-218C at Q. 84-85, 88, 90-91; RX-219C at Q. 79-82.)

Zoran claims that Freescale's infringement claims against the Zoran products were actually litigated in the 709 Investigation, as Freescale filed a complaint, conducted discovery, and participated in a trial. Zoran states that while the accused products in the 709 Investigation were Funai TVs using the Zoran integrated circuit products, there was no allegation or finding that any component in the Funai TVs other than the Zoran products was relevant to the infringement analysis. (Citing JX-55C at 54-66; RX-192C at 34, 65-101.) Zoran claims that the issue decided in the 709 Investigation was whether the Zoran products themselves infringed claims 9 and 10 of the '455 patent. (Citing JX-55C at 54-55.)

Zoran argues that the resolution of the infringement issue was essential to the final determination in the 709 Investigation. Zoran states that the key individual finding upon which the conclusion of no violation was based was the finding that Freescale failed to show that claims 9 or 10 of the '455 patent are infringed. (Citing JX-55C at 105.)

Zoran asserts that Freescale had a full and fair opportunity to litigate the infringement issue in the 709 Investigation. Zoran states that Freescale obtained discovery from both Funai

and Zoran in the 709 Investigation. Zoran states that Freescale offered an expert report on infringement of the Zoran products. Zoran states that Freescale had the opportunity to prove infringement of the Zoran products at trial. Therefore, Zoran argues that it cannot be disputed that Freescale had a full and fair opportunity in the 709 Investigation to litigate the infringement issue.

Freescale's Position: Freescale contends that Zoran failed to prove that issue preclusion applies in this investigation.

Freescale argues that the "essentially the same" test relied on by Zoran is only relevant to claim preclusion, and not issue preclusion. According to Freescale, issue preclusion is a much narrower doctrine that does not have such a broad inquiry.

Freescale argues that issue preclusion cannot apply because it did not have a full and fair opportunity to litigate the issues in the 709 Investigation. Freescale asserts that Funai delayed in providing discovery regarding the third-party suppliers (which included Zoran), and then forced Freescale to obtain all of the discovery from the third parties. Freescale argues that Funai's dilatory tactics prevented Freescale from obtained full discovery regarding the Zoran products so that Freescale could present a complete infringement case.

Freescale notes that issue preclusion is discretionary and subject to equitable considerations. Freescale claims that the equities weigh in favor of not applying issue preclusion in this instance.

Freescale asserts that Chief Judge Luckern's evidentiary ruling in the 709 Investigation was incorrect because Zoran has now admitted that the datasheets and schematics at issue in the 709 Investigation are indeed authentic and reliable. (Citing CX-307C.) Freescale argues that applying issue preclusion would reward the dilatory discovery tactics of Funai in the 709

Investigation. Finally, Freescale argues that applying issue preclusion would create a windfall for Zoran, and that expediency would not be served by applying issue preclusion.

Staff's Position: Staff contends that Freescale's claims against Zoran are precluded in part by the doctrine of issue preclusion.

Staff asserts that the issues between this investigation and the 709 Investigation are identical, and that the infringement issue was already litigated. Staff argues that preclusion applies to both the Zoran products that are identical to the ones adjudicated in the 709 Investigation, and the products that are essentially the same as the adjudicated products. Staff asserts that there is no dispute that the remaining Zoran Resistor Termination Circuit Products are essentially the same as the adjudicated devices. (Citing RX-218C at Q. 90-91; RX-219C at Q. 23-28, 79-81; CX-401C at Q. 186-188.)

Staff states that the resolution of the infringement issue was essential to the final determination of the 709 Investigation. According to Staff, the finding of no violation in the 709 Investigation was premised solely upon the finding that Freescale had failed to prove infringement.

Staff asserts that Freescale had a full and fair opportunity to litigate the infringement issue in the 709 Investigation. Staff notes that Order No. 7 already addressed this issue and found that Freescale had a full and fair opportunity to litigate in the 709 Investigation.

Discussion and Conclusions: Based on the evidence in the record, I find that Freescale is precluded from asserting infringement of claims 9 and 10 of the '455 patent against the following Zoran chips: ZR39770BGCF; ZR39772HGCF-B; ZR39775HGCF-B; ZR39775HGCF-TC; ZR39775HGCF-TC-LP; ZR39785HGCF-B; ZR39787HGCF; and ZR39787HGCF-LP.

The Federal Circuit explained issue preclusion in the following manner:

> Under the doctrine of issue preclusion, also called collateral estoppel, a judgment on the merits in a first suit precludes relitigation in a second suit of issues actually litigated and determined in the first suit. Issue preclusion operates only if: (1) the issue is identical to one decided in the first action; (2) the issue was actually litigated in the first action; (3) resolution of the issue was essential to a final judgment in the first action; and (4) the party against whom estoppel is invoked had a full and fair opportunity to litigate the issue in the first action.

Innovad Inc. v. Microsoft Corp., 260 F.3d 1326, 1334 (Fed. Cir. 2001) (citations omitted). While Zoran was not a party to the 709 Investigation, it still may assert that issue preclusion applies, as "[i]ssue preclusion does not require identical parties; preclusion may be invoked in a case involving the same plaintiff and either a party or a non-party to the first action." *Id.*

Identical Issues

The first factor to address is whether or not "the issue is identical to one decided in the first action." While Funai was the named respondent, Freescale's infringement allegations were directed to Zoran chips that were found in Funai televisions. (JX-55C at 55.) The following eight Zoran chips were accused of infringement in the 709 Investigation and have been accused of infringement in this investigation: ZR39770BGCF; ZR39772HGCF-B; ZR39775HGCF-B; ZR39775HGCF-TC; ZR39775HGCF-TC-LP; ZR39785HGCF-B; ZR39787HGCF; and ZR39787HGCF-LP. (*See id.*; RX-218C at Q. 87.) There is no dispute between the parties that the issue of whether or not these eight Zoran chips infringe claims 9 or 10 of the '455 patent was decided in the 709 Investigation. (CIB at 63-68.) Therefore, I find that the issue of infringement for these eight products is identical to the infringement issue decided in the 709 Investigation.

Zoran argues that the accused chips that are essentially the same as the above-listed chips are also subject to issue preclusion. I do not concur. Nowhere in the issue preclusion analysis

described *supra* does the Federal Circuit state that issue preclusion applies to products that are "essentially the same" as products adjudicated in the first action.

Zoran cites two cases in support, but neither case dictates the result argued by Zoran. (ZRB at 10-11.) Zoran claims that the Federal Circuit applied the "essentially the same" test when analyzing issue preclusion in *Nystrom v. Trex Co.*, 580 F.3d 1281, 1285 (Fed. Cir. 2009). While the Federal Circuit applied the "essentially the same" test in *Nystrom*, it came in the context of claim preclusion, which is a different doctrine than issue preclusion. *Id.*; *see also Sharp Kabushiki Kaisha v. Thinksharp, Inc.*, 448 F.3d 1368, 1370 (Fed. Cir. 2006) (noting the difference between claim preclusion and issue preclusion). Importantly, claim preclusion requires that "the parties are identical or in privity." *Ammex, Inc. v. United States*, 334 F.3d 1052, 1055 (Fed. Cir. 2003). Because Zoran was not a party in the 709 Investigation and is not in privity with Funai, claim preclusion does not apply.

Zoran also cites *Aspex Eyewear, Inc. v. Marchon Eyewear, Inc.*, 672 F.3d 1335, 1343 (Fed. Cir. 2012) to support its argument. In citing *Aspex*, Zoran focuses on the following passage:

> In arguing to the contrary, Revolution relies on this court's decision in *Nystrom v. Trex Co.*, 580 F.3d 1281, 1285–86 (Fed.Cir.2009), to support its claim that res judicata bars Aspex's claims in this case. The *Nystrom* court held that particular claims were barred based on previous litigation between the same parties. The previous litigation in that case, however, had resolved certain issues against the appellant, and the appellant sought to litigate those issues again in the second case, hoping for a different outcome. Because those issues had been resolved against the appellant in the first case, this court held that the appellant was precluded from relitigating them. In so doing, the court applied the doctrine generally referred to as collateral estoppel or issue preclusion. Although the *Nystrom* court characterized its analysis as falling under the general rubric of res judicata or claim preclusion, the principle that the court applied was that when a party that has had a full and fair opportunity to litigate an issue and has lost on that issue, it may not relitigate that issue in a later case.

Aspex, 672 F.3d at 1343.

I find that the *Aspex* court's characterization of the analysis in *Nystrom* is not a sufficient basis to conclude that the "essentially the same" test should apply to Zoran's issue preclusion argument. The court in *Nystrom* is clear that it is applying claim preclusion to a second lawsuit brought against a party that was a named defendant in the first suit. *See Nystrom*, 580 F.3d 1284-1285. Because claim preclusion requires that the parties in both suits be identical, ***claim preclusion cannot apply in the case at bar***. *Ammex*, 334 F.3d at 1055. Here, Zoran is seeking to apply ***issue preclusion***, which expressly requires that "the issue is ***identical*** to one decided in the first action." *Innovad*, 260 F.3d at 1334 (emphasis added).

Actually Litigated

The second factor looks at whether or not "the issue was actually litigated in the first action." I find that the issue of whether or not the eight above-named Zoran chips infringe claims 9 and 10 of the '455 patent was actually litigated in the 709 Investigation. Chief Judge Luckern performed a full infringement analysis for the eight Zoran chips, ultimately concluding that Freescale "has failed to show that asserted claims 9 and 10 of the '455 patent are infringed." (*See* JX-55C at 36-66, 105.) Freescale does not dispute that this factor is met. (CIB at 63-68.)

Resolution Was Essential To A Final Judgment

The third factor looks at whether or not "resolution of the issue was essential to a final judgment in the first action." I find that resolution of the infringement issue was essential to a final judgment in the 709 Investigation, as the finding of no violation of Section 337 was premised on Chief Judge Luckern's conclusion that Freescale failed to prove that the Funai televisions incorporating the accused Zoran chips infringed claims 9 or 10 of the '455 patent. (JX-55C at 105.) Freescale does not dispute that this factor is met. (CIB at 63-68.)

Full & Fair Opportunity To Litigate

The fourth and final factor looks at whether or not "the party against whom estoppel is invoked had a full and fair opportunity to litigate the issue in the first action." I find that Freescale had a full and fair opportunity to litigate the infringement issue in the 709 Investigation.

Freescale argues that it did not receive a full and fair opportunity to litigate due to Funai's dilatory tactics in discovery. Specifically, Freescale asserts that Funai delayed in identifying the chips found in its television products, and then delayed in informing Freescale that it did not possess the relevant technical documents regarding the Zoran chips. According to Freescale, Funai's tactics in discovery prevented Freescale from obtaining the discovery it needed from Zoran to present a complete case. Freescale asserts that the "[f]inality of the Zoran documents was only an issue in the 709 Investigation because Funai's dilatory tactics succeeded in delaying production of Zoran's technical information until it was too late." (CIB at 66.)

In the 709 Investigation, Chief Judge Luckern found that Freescale failed to establish the finality[6] and reliability of the Zoran technical documents that Freescale relied on to prove infringement. (JX-55C at 36-54.) While Freescale was able to obtain the Zoran documents during discovery through a third party subpoena to Zoran, Freescale did not offer any testimony at the hearing from a Zoran witness to demonstrate the finality and reliability of the documents. (*Id.*) Instead, Freescale relied on its expert, Dr. Subramanian, as the sponsoring witness for the documents. (*Id.*) Chief Judge Luckern made clear that Freescale was given an opportunity to depose Zoran regarding the documents, and chose not to do so:

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[6] The finality of the Zoran documents was an issue because certain documents included statements that the information contained in the document was preliminary in nature. (*See, e.g.,* JX-55C at 40.)

> It is a fact that complainant did not depose Zoran. However, it is also a fact that the administrative law judge issued a subpoena ad testificandum and duces tecum to Zoran Corporation as early as July 9, 2010, nearly six months before the beginning of the evidentiary hearing...Further, in Order No. 19, the administrative law judge extended the fact discovery deadline to October 8, 2010, to allow, inter alia, complainant to complete discovery with respect to Zoran "including concluding document production and providing a witness to testify." (Order at 1.) Said extension of discovery occurred approximately four months before the beginning of the evidentiary hearing.

(JX-55C at 45, n. 10.)

Based on the foregoing, I find that there is no support for Freescale's claim that Funai's tactics prevented Freescale from obtaining the necessary discovery it needed from Zoran. Furthermore, any complaints regarding discovery misconduct on the part of Funai should have been raised by Freescale in the 709 Investigation, and not now.

Whether or Not Issue Preclusion Should Apply

Finally, Freescale argues that even if each of the four above-described factors is satisfied, I should decline to apply issue preclusion due to equitable considerations. (CIB at 66-68.) The Commission has explained that "[t]he application of issue preclusion is discretionary and the court must determine if its application is appropriate in view of any equitable considerations." *Certain Semiconductor Integrated Circuits Using Tungsten Metallization & Products Containing Same*, Inv. No. 337-TA-648, Comm'n Op. at 3 (Feb. 18, 2009). I find no reason why equitable considerations should preclude the application of issue preclusion in this instance. After reviewing the arguments put forth by Freescale, I find that application of issue preclusion would not unfairly penalize Freescale or unfairly benefit Zoran. To put it simply, Freescale had the opportunity to prove infringement of these eight Zoran products in the 709 Investigation, and it failed to do so. I find no justification for allowing Freescale a second chance at proving infringement.

After a review of the four issue preclusion factors, it is clear that Zoran has demonstrated that issue preclusion shall apply to the products that were actually adjudicated in the 709 Investigation. I find that Freescale is precluded from asserting infringement of claims 9 and 10 of the '455 patent against the following Zoran chips: ZR39770BGCF; ZR39772HGCF-B; ZR39775HGCF-B; ZR39775HGCF-TC; ZR39775HGCF-TC-LP; ZR39785HGCF-B; ZR39787HGCF; and ZR39787HGCF-LP.

VI. INFRINGEMENT

A. Applicable Law

A complainant must prove either literal infringement or infringement under the doctrine of equivalents. Infringement must be proven by a preponderance of the evidence. *SmithKline Diagnostics, Inc. v. Helena Labs. Corp.*, 859 F.2d 878, 889 (Fed. Cir. 1988). A preponderance of the evidence standard "requires proving that infringement was more likely than not to have occurred." *Warner-Lambert Co. v. Teva Pharm. USA, Inc.*, 418 F.3d 1326, 1341 n. 15 (Fed. Cir. 2005).

Literal infringement is a question of fact. *Finisar Corp. v. DirecTV Group, Inc.*, 523 F.3d 1323, 1332 (Fed. Cir. 2008). Literal infringement requires the patentee to prove that the accused device contains each and every limitation of the asserted claim(s). *Frank's Casing Crew & Rental Tools, Inc. v. Weatherford Int'l, Inc.*, 389 F.3d 1370, 1378 (Fed. Cir. 2004).

As for the doctrine of equivalents:

> Infringement under the doctrine of equivalents may be found when the accused device contains an "insubstantial" change from the claimed invention. Whether equivalency exists may be determined based on the "insubstantial differences" test or based on the "triple identity" test, namely, whether the element of the accused device "performs substantially the same function in substantially the same way to obtain the same result." The essential inquiry is whether "the accused product or process contain elements identical or equivalent to each claimed element of the patented invention[.]"

TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc., 529 F.3d 1364, 1376-77 (Fed. Cir. 2008) (citations omitted).

Thus, if an element is missing or not satisfied, infringement cannot be found under the doctrine of equivalents as a matter of law. *London v. Carson Pirie Scott & Co.*, 946 F.2d 1534, 1538-39 (Fed. Cir. 1991). Determining infringement under the doctrine of equivalents "requires an intensely factual inquiry." *Vehicular Techs. Corp. v. Titan Wheel Int'l, Inc.*, 212 F.3d 1377, 1381 (Fed. Cir. 2000).

B. MediaTek

Freescale's Position: Freescale has accused four groups of MediaTek integrated circuits of infringing claims 9 and 10 of the '455 patent: {

} (collectively the "Accused MediaTek Products"). According to Freescale, each is a packaged integrated circuit that serves as a controller chip in digital televisions. (Citing CX-401C at Q.64.) Freescale contends that each of the listed integrated circuits within {

} (Citing CX-401C at Q.63, 65.) Freescale contends that MediaTek's expert witness, Dr. Knox, testified that the Accused MediaTek Devices in {

} for purposes of analyzing infringement of claims 9 and 10 of the '455 patent. (Citing Tr. at 470:7-16.)

Freescale asserts that each Accused MediaTek Product includes "a data processor within an integrated circuit package." According to Freescale, Dr. Knox agrees that the Accused

MediaTek Products meet this limitation and has not offered an opinion to the contrary. (Citing Tr. at 500:16-23.)

Freescale asserts that each Accused MediaTek Product includes "an execution unit internal to the data processor," which the parties agree should be construed to mean "a portion of an integrated circuit that executes commands or instructions." According to Freescale, Dr. Knox agrees that the Accused MediaTek Products meet this limitation and has not offered an opinion to the contrary. (Citing Tr. at 500:24-501:3.)

Freescale asserts that each Accused MediaTek Product includes "a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus." As an example, Freescale contends that {

} (Citing CX-104C at MTK 688, 700-01; CX-105C at MTK 805-06, 818-19; JX-10C at Vol. 1, 19:21-20:22; CX-401C at Q. 80.) According to Freescale, Dr. Knox agrees that the Accused MediaTek Products meet this limitation. (Citing Tr. at 501:4-502:17.)

Freescale asserts that the Accused MediaTek Products meet the "plurality of bus termination circuits providing data to or receiving data from the execution unit" limitation. (Citing CX-401C at Q. 83-84, 109-10, 136-37, 162-63.) According to Freescale, {

}

{ }

(Citing *id.*; JX-10C at Vol. 1, 40:16-41:21, Vol. 2, 104:23-111:21.) Freescale asserts that the{

}

Freescale asserts that the Accused MediaTek Products meet the limitation "each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal." (Citing CX-401C at Q. 85, 111, 138, 164.) According to Freescale, {

}

Freescale asserts that the Accused MediaTek Products meet the limitation "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the

plurality of external pins wherein each external pin is coupled to at least one bus termination circuit." Freescale contends that it and Staff have proposed that "bus termination circuit" be construed to mean "circuitry for signal termination that is selectively enabled or disabled in response to [a] control signal whose assertion is based, at least in part, on the direction of data signals on the bus." According to Freescale, respondents construe this term as "circuitry for signal termination that is selectively enabled or disabled in response to a control signal."

Freescale asserts that each Accused MediaTek Product includes "a plurality of bus termination circuits" under either Freescale's/Staff's construction or Respondents' construction of "bus termination circuit." (Citing CX-401C at Q. 82, 108, 135, 161.) According to Freescale, {

} (Citing JX-10C at Vol. 1, 16:2-5, 16:24-17:16, Vol. 2, 104:23-111:21, 111:24-112:20.) {

} (Citing JX-10C at Vol. 1, 17:17-20.) Freescale contends that {

}

Freescale contends that {

} is a "bus termination circuit" under either proposed construction for this term, as are the { } in Groups II-IV. (Citing CX-401C at Q. 82, 108, 135, 161.) Freescale asserts that {

} (Citing CX-401C at Q. 82, 108, 135, 161; JX-10C at Vol. 1, 24:11-25:15, 26:16-27:23, Vol. 2, 104:23-111:21.) As an example, Freescale explains that, { }

{

}

{

} (Citing JX-10C at Vol. 1, 29:12-31:10; Tr. at 478:1-12.) According to Freescale, because these signals "selectively enable or disable" circuitry for signal termination "in response to [a] control signal," they are "control signals" as required by Respondents' proposed construction for "bus termination circuit." (Citing CX-401C at Q. 82, 108, 135, 161.)

In its reply brief, Freescale asserts that MediaTek's expert testified that: (1)

{

}

Freescale asserts that the Accused MediaTek Products meet the "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus

termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus" claim limitation.

{

}

152C; CX-401C at Q. 114, 141, 167; Tr. at 473:1-474:10.)

Freescale asserts that the {

} (Citing CX-136C; CX-132C; CX-134C; CX-145C; CX-142C; CX-140C; CX-163C; CX-158C; CX-161C; CX-401C at Q. 89-90, 115-116, 142-43.) According to Freescale, in each {

} (Citing *id.*)

According to Freescale, when the gate control G is brought to logic low or 0, the p-channel transistor is turned on and the impedance across {

}

{

}

Freescale asserts that even if the claim term "a conductor" is limited to a single conductor as argued by respondents, Dr. Subramanian identified such a conductor. According to Freescale,

{

}

Freescale asserts that MediaTek's arguments mischaracterize the express language of

claim 9, manufacturing a limitation that the control signal of claim 9 must be the sole, necessary and sufficient cause of the enabling and disabling of termination. Freescale asserts that claim 9, by its express language, imposes no such limitation, reciting only that the control signal "allows" coupling and decoupling of circuit components without imposing limitations on whether other signals contribute to effectuating the coupling and decoupling allowed by the control signal of claim 9. According to Freescale, Dr. Knox testified that {

} (Citing Tr. at 477:15-22.) Freescale contends that MediaTek's reading, in effect, requires that the control signal pass through a continuous conductor, all the way to the individual transistors that couple or decouple termination, without undergoing any intermediate logical operations within the termination circuitry. (Tr. at 529:4-17.) According to Freescale, Dr. Knox acknowledges that nothing in the plain language of claim 9 explicitly imposes such a limitation. (Tr. at 530:13-531:3.) Freescale asserts that each accused {

}

(Citing *id.* at 498:2-6.)

Freescale contends that even if claim 9 is read to require a control signal that operates without contribution from other signals, the Accused MediaTek Products still infringe because the control signals taken together are sufficient to couple and decouple circuit components from the bus. (Citing CX-401C at Q. 82.) According to Freescale, Dr. Knox testified that {

}

{

} but simply construes claim 9 to exclude systems in which multiple conductors carry the same signal to each termination circuit. According to Freescale, such a reading is at odds with the claim language, which uses different terms to refer to "a conductor" for each termination circuit and "the control signal" carried by the conductor, indicating that the two are not synonymous, and that each termination circuit can receive the control signal via its own conductor. Freescale contends that the indefinite article "a," when used in patent claims, means one or more. (Citing *Tate Access Floors, Inc. v. Interface Architectural Res., Inc.*, 279 F.3d 1357, 1370 (Fed. Cir. 2002).) According to Freescale, Dr. Knox admits that {

}

Freescale disagrees with MediaTek's argument that its products do not include "a conductor coupled to each input of each of the bus termination circuits" because {

} (Citing RX-221C at Q. 155; MPHB.) According to Freescale, nothing in the plain language of claim 9 excludes intermediate processing of the control signal. Freescale asserts that the claim merely requires that the control signal allow coupling and decoupling of a circuit component from the bus, not that the control signal pass, unprocessed via a continuous conductor to the individual termination circuits. Freescale contends that Dr. Knox testified that nothing in the plain language of claim 9 requires that the conductor pass the control signal, unprocessed, through a continuous conductor to the transistor gates by which a circuit component is coupled or

decoupled. (Citing Tr. at 530:7-531:3.) As a result, Freescale concludes that MediaTek's reading of claim 9 requires limitations not found in the claim language and should be rejected.

{

} (Citing JX-10C at Vol. 1, 56:1-58:16, 59:7-60:25, 61:8-15; CX-401C at Q. 82; Tr. at 351:24-352:22, 476:20-23, 478:19-479:14.)

In its reply brief, Freescale also asserts that MediaTek wrongly contends that Dr. Subramanian has changed positions regarding whether or not other signals labeled { } also constitute the control signal under Respondents' construction. (Citing MIB at 36.) Freescale contends that Respondents' construction for the term "bus termination circuits" changed, not Dr. Subramanian's understanding of the accused products. (Citing MIB at 37.) According to Freescale, Dr. Subramanian testified that the { } constitute the claimed control signals under his reading of the claims as well as Respondents former construction of "bus termination circuit." (Citing CX-401C at Q. 82.)

Freescale asserts that the Accused MediaTek Products infringe claim 10 of the '455 patent. According to Freescale, in the Accused MediaTek Products "at least one circuit

component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, an electrical short circuit, and an inductor." Freescale contends that the {

} (Citing CX-401C at Q. 93-96; Tr. at 484:11-485:1, 492:20-493:6, 494:12-17.) As a result, Freescale asserts that the Group I Accused MediaTek Devices practice the limitations of claim 10. (Citing *Id.*)

MediaTek's Position: MediaTek asserts that the Accused MediaTek Products do not have "bus termination circuits" under the parties' agreed construction. MediaTek asserts that it was undisputed at the hearing that { } that Freescale accuses as the "bus termination circuits" of claim 9 include substantial structures and circuitry that have nothing to do with bus termination. (Citing Tr. at 275:24–276:20; RX-221C at Q. 206, 211–214; CX-401C at Q. 87.) MediaTek contends that regardless of the "comprising" preamble of the claim, Freescale must properly identify structures that actually match the construed claim terms in order to carry its burden of proving infringement. (Citing *Genentech, Inc. v. Chiron Corp.*, 112 F.3d 495, 501 (Fed. Cir. 1997).)

MediaTek separately asserts that a particular version of the { } (one of the Accused MediaTek Products) {

} (Citing RX-221C at Q. 155, 221–224.) According to MediaTek, this particular version of the { } does not infringe claims 9 and 10 of the '455 patent for the additional reason that it { } and therefore does not have a "bus termination circuit" or a "control signal [that], when asserted, allows each bus

---

[7] { }

termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus." (Citing *id.*; Tr. at 483:15–484:10; RX-221C at Q. 155.)

MediaTek asserts that if the term "a conductor coupled to each input of each of the bus termination circuits" is construed to require a single or common conductor, it is undisputed that the Accused MediaTek Products do not infringe the asserted claims. (Citing Tr. at 259:17-261:8.) According to MediaTek, claim 9 requires that there must be at least one conductor that meets the claim limitations, i.e., at least one conductor that provides one "control signal" capable of providing the claimed coupling and decoupling functionality. (Citing JX-1 at 10:45–53; RX-221C at Q. 164.) MediaTek asserts that Dr. Subramanian's infringement opinion is incorrect because { } does not constitute a single (i.e., common) conductor that carries "the control signal" as required by claim 9. According to MediaTek, its products, therefore, do not infringe claims 9 and 10 of the '455 patent. (Citing RX-221C at Q. 156–58.)

MediaTek asserts that claim 9 requires that there must be at least *one* conductor that meets the claim limitations, *i.e.,* at least *one* conductor that provides *one* "control signal" capable of providing the claimed coupling and decoupling functionality. (Citing JX-1 at 10:45–53; RX-221C at Q. 164.) MediaTek asserts that Dr. Subramanian's infringement opinion is incorrect because { } does not constitute a single (*i.e.,* common) conductor that carries "the control signal" as required by claim 9. According to MediaTek, its products, therefore, do not infringe claims 9 and 10 of the '455 patent. (Citing RX-221C at Q. 156–58.)

MediaTek asserts that the structure that Freescale identifies as the accused "bus termination circuits" constitutes { } for each of the data lines on a data bus. (Citing Tr. at 264:6–25; CX-138C at MTK-786-ITC-00036536; RX-59C.087 at MTK-786-ITC-00036536.) According to MediaTek, the {

} (Citing RX-221C at Q. 91; Tr. at 497:3-7; RX-222C at Q. 25-26.) MediaTek asserts that there is no single or common conductor coupled to "each input" of the accused "bus termination circuit."

MediaTek contends that Freescale's expert, Dr. Subramanian, accuses {

} of being the "control signal" of claim 9. (Citing Tr. at 267:15–20; CPHB at 37–38.) According to MediaTek, Dr. Subramanian asserts that the accused seven inputs, collectively ***or*** individually, perform the required function of coupling/decoupling the circuit components from the bus. (Citing Tr. at 267:21–25.)

MediaTek asserts that the { } identified by Dr. Subramanian cannot collectively couple a circuit component to the bus because {

}

{

}

197.) MediaTek asserts that this testimony stands un-rebutted by Dr. Subramanian.

MediaTek asserts that none of the seven signals identified by Freescale individually can perform the function required by claim 9. According to MediaTek, Dr. Subramanian initially contended that {

} satisfy the functional requirement for the claim 9 control signal. (Citing CX-401C at Q. 85, 87; Tr. at 267:21–25.) MediaTek asserts that on cross-examination Dr. Subramanian admitted that there {

} (Citing *id.*)

{

} MediaTek contends that although Dr. Subramanian initially contended that

{ } each met the requirements of claim 9 (Citing Tr. at 267:15–25), on cross-

examination Dr. Subramanian backed down from this contention. According to MediaTek, Dr. Subramanian admitted that the { } individually do not have the ability to couple a circuit component to the bus. (Citing Tr. at 275:17–23.) MediaTek contends that Dr. Subramanian also admitted that under his construction of the term "bus termination circuit" the { } ***cannot*** be the claimed control signal for any of the Accused MediaTek Products, because they are not based at least in part on the direction of data signals on the bus. (Citing Tr. at 270:8–271:15.)

MediaTek asserts that Dr. Knox has provided a detailed explanation regarding why the { } have neither the ability nor the authority to couple circuit components to the bus. (Citing RX-221C at Q. 194.) According to MediaTek, Dr. Knox explained that each of the {

}

MediaTek asserts that Dr. Knox opined that the agreed-upon construction for the term "bus termination circuit" requires "a control signal whose assertion is based, at least in part, on the direction of data signals on the bus." (Citing JSRCC at Ex. A; RX-221C at Q. 212.) {

} (Citing Tr. at 270:8–271:15; RX-221C at Q. 194; CX-401C at Q. 82, 108, 135, 161.)

MediaTek contends that Dr. Knox opined that the alleged "circuit components" (resistors) can be coupled to or decoupled from the bus {

} (Citing RX-221C at Q. 194.) MediaTek asserts that Freescale clearly cannot

carry its burden of satisfying the "control signal" limitation with these { } (Citing Tr. at 270:8–271:15, 275:17–23.) MediaTek asserts that signal {

} According to MediaTek, because the specific state of the {

} this signal cannot be the "control signal" of claim 9 of the '455 patent. (Citing RX-221C at Q. 197.)

MediaTek contends that the circuitry that Dr. Subramanian accuses as the "bus termination circuit" in MediaTek's products has {

} (Citing Tr. at 274:23–275:7; RX-221C at Q. 197.) As a result, MediaTek concludes that the specific state of the { } bears no correlation to whether circuit components are coupled to or decoupled from the bus.

MediaTek asserts that Dr. Subramanian conceded that the { } on its own, cannot

couple a circuit component to the bus. (Citing Tr. at 268:9–24.) According to MediaTek, since the { } cannot meet the requirements of claim 9. (Citing RX-221C at Q. 197.) MediaTek asserts that Dr. Knox has provided a detailed explanation for why the { } has no correlation to whether circuit components are coupled to the bus, and why, therefore, it cannot meet the "control signal" requirements of claim 9. (Citing RX-221C at Q. 195–202.)

In its reply brief, MediaTek disagrees with Freescale's statement that { } (Citing RX-221C at Q. 99, 105, 144, 171, 195–97; Tr. at 129:23–130:13, 131:17–132:9, 134:9–12, 134:22–135:2, 274:10–275:7, 353:15–18, 544:1–11.)

MediaTek asserts that Freescale waived any argument that Accused MediaTek Products infringe claim 9 under MediaTek's construction of "a conductor" pursuant to Ground Rule 8.2. According to MediaTek, Freescale's pre-trial brief disclosed no such theories, and Freescale is therefore barred from making them now. (Citing CIB at 14–33; G.R. 8.2.) MediaTek also

asserts that Freescale could not, and did not, carry its burden of proving infringement under Respondents' or the Staff's claim constructions of the "a conductor..." claim term. According to MediaTek, the seven conductors accused by Freescale are not a single or common conductor.

MediaTek asserts that claim 9 requires a plurality of bus termination circuits, with "each external pin [] coupled to at least one bus termination circuit." (Citing JX-1 at 10:34–38.) According to MediaTek, its construction of the "a conductor ..." term require a single conductor coupled to each of the bus termination circuits on the different lines of the bus. (Citing RX-221C at Q. 33.) MediaTek asserts that Freescale presented no evidence {

}

In its reply brief, MediaTek asserts that Freescale improperly introduces a new theory that a signal can be "the control signal" of claim 9 so long as it "shares control" or "contribute[s] to effectuating the coupling and decoupling allowed by the control signal of claim 9." (Citing CIB at 29, 30.) According to MediaTek, Freescale has consistently alleged that the "control signals" it accuses have the ability to, and do in fact, couple the accused circuit components to the bus, either individually or collectively. (Citing CPHB at 37 ("These control signals, when asserted, ***couple*** at least one circuit component . . . to the bus . . . ."); CIB at 24.) MediaTek asserts that Freescale never mentioned in its pre-trial brief or witness statements its theory that a

signal satisfies the "control signal" limitation of claim 9 if it "shares control" or "contribute[s] to effectuating the coupling and decoupling allowed by the control signal of claim 9." (Citing CIB at 29, 30; CPHB; CX-401C.) According to MediaTek, Freescale waived this theory under Ground Rule 8.2.

MediaTek asserts that Freescale's theory that a "control signal" of claim 9 can be "processed" in combination with other non-accused signals, so long as at some point an actual signal does couple a circuit component to the bus, should be rejected. (Citing CIB at 32 ("nothing in the plain language of claim 9 excludes intermediate processing of the control signal").) MediaTek asserts that Freescale's argument that an accused signal can be "processed" along with other signals to generate a new and different signal that actually couples a bus termination circuit to the bus was also waived under Ground Rule 8.2.

MediaTek asserts that waiver aside, Freescale's theory fails for several reasons. First, MediaTek contends that the evidence is undisputed that {

}

MediaTek asserts that "shar[ing] control" and "contribut[ing] to effectuating the coupling and decoupling allowed by the control signal of claim 9" would seem to have nearly limitless application. MediaTek contends that a power signal turning the IC chip on and off would appear to qualify as a "control signal" under this amorphous standard. According to MediaTek, such an

open-ended application of the "control signal" limitation would not only violate 35 U.S.C. § 112, Second Paragraph, but would also destroy the public notice function of the '455 patent claims. (Citing *PSC Computer Prods., Inc. v. Foxconn Int'l, Inc.*, 355 F.3d 1353, 1359–60 (Fed. Cir. 2004).)

MediaTek asserts that Freescale's "share or contribute" infringement theory attempts to back-door Order 21 and rulings during the hearing that excluded the { } by arguing that the seven control signals it has properly accused, in some combination with signals such as { } "allow" a circuit component to be coupled to the bus.

MediaTek asserts that Freescale's "share or contribute" theory is really a doctrine of equivalents theory. According to MediaTek, Freescale is taking the position that an accused signal does not have to allow a circuit component to be coupled to the bus, but instead only has to "share with" or "contribute to" signals that do allow the circuit component to be coupled to the bus. MediaTek asserts that this is an argument that the accused signals are "substantially equivalent" to the claimed "control signal" of claim 9 and Freescale waived the right under Ground Rule 8.2 to make any such contentions.

MediaTek asserts that Freescale's "share or contribute" theory is contrary to positions Freescale and its expert have taken in this litigation. MediaTek asserts that Freescale's expert has consistently interpreted the required function of the "control signal" of claim 9 as requiring that the control signal "couple at least one circuit component . . . to the bus." (Citing CX-401C at Q. 86, 87, 113, 140, 166, 202, 227, 251.) MediaTek contends that Dr. Subramanian has steadfastly maintained that the "control signal" of claim 9 corresponds to the ENABLE signal of the '455 patent, which is also inconsistent with Freescale's new "share or contribute to" theory. (Citing Tr. at 218:23–220:7, 241:13–243:2.) According to MediaTek, figure 1 of the '455 patent

shows three non-data signals identified by name in device 10: ENABLE, MASTER/SLAVE* (M/S) and INTERNAL R/W* (R/W). (Citing JX-1 at 3:5–30, 4:40–50, 4:63–5:32.) MediaTek asserts that under Freescale's "share or contribute" theory, the M/S or R/W signals would qualify as the "control signal" claimed in claim 9, although neither signal has the ability or authority to couple a circuit component to the bus.

MediaTek asserts that Freescale argues the Accused MediaTek Products infringe claim 9 regardless of whether the signals that Freescale actually accuses qualify as the "control signal" of claim 9 under the logic that there are signals that allow { } According to MediaTek, the { } which was not accused by Freescale. MediaTek asserts that Freescale's attempt to accuse a new signal that was never mentioned in Freescale's pre-trial brief is a blatant violation of Ground Rule 8.2.

MediaTek asserts that, waiver notwithstanding, the conductor carrying the { } is not "a conductor coupled to each input" of the bus termination circuits, or "a conductor coupled to ... each of the bus termination circuits" as required by claim 9 because the {

}

Staff's Position: Staff asserts that the Accused MediaTek Products do not include "bus termination circuits" as construed by Freescale. Staff asserts that none of the signals identified as "control signals" in the { } can satisfy the "control signal" portion of Freescale's construction of "bus termination circuits" because the signals are not based on the direction of the data. (Citing Tr. at 271:5-15.) Moreover, Staff contends that multiple blocks of circuitry exist between the { } in the Accused

MediaTek Products and the {

}

Staff asserts that Freescale now recognizes that its "control signal" infringement theory is factually inaccurate for MediaTek's products. According to Staff, with respect to {

}as required by the agreed construction of "bus termination circuit"—and therefore cannot be the accused control signals. (Citing Tr. at 270:19–24, 271:5–15.)

In its reply brief, Staff asserts that Freescale contends that {

} constitute the claimed "control signal" and the claimed "a conductor." (Citing CIB at 24.) According to Staff, the evidence is uncontested that these seven signals, {

} (Citing RX-221C at Q. 170.) Staff asserts that Dr. Knox explained that "in order for a signal to allow a circuit component to be coupled to the bus, it must have the ability or authority to couple that component to the bus." (Citing *id.* at Q. 194, 197.) According to Staff, this testimony stands un-rebutted by Dr. Subramanian.

Discussion and Conclusions: Based on the evidence in the record, I find that Freescale has failed to demonstrate by a preponderance of the evidence that the Accused MediaTek

Products meet the claim 9 limitations that require "a plurality of bus termination circuits" and "wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus."

First, Freescale has not met its burden to prove by a preponderance of the evidence that the Accused MediaTek Products include "a plurality of bus termination circuits." The evidence introduced by Freescale fails to establish that the four groups of Accused MediaTek Products include "bus termination circuits." Freescale's infringement allegations assert that the { } Accused MediaTek Products is a "bus termination circuit," as required by claim 9 and { } is a control signal based on the direction of data signals that selectively enables or disables circuitry for signal termination as required by the parties' agreed claim construction for "bus termination circuit." (*See* CIB at 19-22.) As explained below, however, the evidence introduced at the hearing shows that {

}

Pursuant to Order No. 21, Freescale is not permitted to assert that { } are "control signals." In Order No. 21, I struck the portions of Dr. Subramanian's initial expert report that referred to { } as "control signals" because Freescale failed to identify those signals as control signals in response to MediaTek's contention interrogatory concerning infringement.

MediaTek's expert testified that a {

} (Tr. at 476:12-

477:23.) MediaTek's expert further testified the {

} (Tr. at 477:15-25.) Thus, the {

} Indeed, Dr. Subramanian, Freescale's expert, admitted that changing the value of {

} (Tr. at 272:8-275:16.) Thus, the accused bus termination circuit is not "selectively enabled or disabled" in ***response*** to the accused { } as required by the parties' agreed construction for "bus termination circuit." Rather, additional inputs are required—inputs that Freescale is not permitted to assert are "control signals." As a result, the {

} of the Accused MediaTek Products do not meet the "bus termination circuit" limitation of claim 9.

One exception exists to the { } of the Accused MediaTek Products. Evidence presented by MediaTek shows that a particular version of {

} (Tr. at 484:5-10.) Freescale did not try to rebut this evidence. As a result, Freescale has failed to meet its burden to show that {

} meets the "a plurality of bus termination circuits" limitation of claim 9.

Freescale also has not met its burden to prove by a preponderance of the evidence that the Accused MediaTek Products meet the claim 9 limitation requiring that "the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus."

Freescale has asserted that certain inputs to the accused bus termination circuit are "control signals" for purposes of this claim limitation—{

} None of these seven alleged "control signals," alone, or collectively, "when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus" and "when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus." Freescale's expert, Dr. Subramanian, admitted that none of the seven alleged "control signals" ***individually*** couple a circuit component to the bus. (Tr. at 269:11-18.) As a result, Freescale has failed to prove by a preponderance of the evidence that any of the seven alleged "control signals" individually are the "control signals" required by claim 9.

Freescale also has failed to tie the coupling and decoupling of circuit components to the bus to the assertion/deassertion of the seven accused "control signals" considered as a whole.

{

}

{

} (Tr. at 531:17-533:4.) Freescale fails, however, to link the seven alleged "control signals" to {

} (*See* CIB 24-28; CRB at 17.)

The evidence introduced at the hearing weighs against finding a link between the seven alleged "control signals" and the coupling and decoupling of circuit components. (*See* Tr. at 542:15-24.) First, as discussed above, {

}

Freescale unpersuasively argues that the alleged "control signals" need only contribute, along with other signals that are not accused of being control signals, to the coupling or decoupling of circuit components to meet this claim limitation. Freescale's argument effectively

---

[8] As argued by counsel for Freescale, "termination circuits" are distinct from the claimed "bus termination circuits." (Tr. at 527:11-25.)

is that { } accomplishes the required functionality—coupling or decoupling of circuit components to the bus. (*See* CIB at 29.) First, this is merely a backdoor argument that { } are themselves "control signals." I cautioned Freescale that backdoor arguments that { } are "control signals" would violate Order No. 21. (*See* Tr. at 28:16-20.) As noted above, Freescale is not permitted to assert that { } are "control signals," and for that reason alone, Freescale's argument fails.

Second, this argument was waived by Freescale. Freescale did not raise this theory of "control signals" merely "contributing" to coupling and decoupling of components to the bus in its prehearing brief. Rather, Freescale's prehearing brief asserted that "control signals, when asserted, couple at least one circuit component, a transistor and one or more resistors, to the bus through the { } (CPHB at 37.) Freescale's prehearing brief did not assert that the control signals "contribute" to coupling of a circuit component, as it now alleges. (*See id.*) Ground Rule 8.2 provides, *inter alia*, "[a]ny contentions not set forth in detail as required herein shall be deemed abandoned or withdrawn, except for contentions of which a party is not aware and could not be aware in the exercise of reasonable diligence at the time of filing the pre-trial brief." As a result, Freescale's arguments that the "control signals" must merely "contribute" to the coupling and decoupling of components to/from the bus to meet this claim limitation were waived.

Based on the record, Freescale has failed to prove by a preponderance of the evidence that the seven accused "control signals" in the Group I Accused MediaTek Products "when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal,

when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus," as required by Claim 9. Because Freescale has elected to {

} (*See* CIB at 15), Groups I-IV of the Accused MediaTek Products do not meet this limitation of claim 9.

Based on the foregoing, I find that Freescale has failed to demonstrate by a preponderance of the evidence that the Accused MediaTek Products infringe asserted claim 9 of the '455 patent. Claim 10 depends from claim 9 and incorporates all claim 9 limitations. As a result, for the same reasons discussed above, Freescale has failed to demonstrate by a preponderance of the evidence that the Accused MediaTek Products infringe asserted claim 10 of the '455 patent. *Wahpeton Canvas Co. v. Frontier, Inc.*, 870 F.2d 1546, 1552 n. 9 (Fed. Cir. 1989) ("One who does not infringe an independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim.")

C. Zoran

Freescale's Position: Freescale has accused three groups of Zoran products of infringing claims 9 and 10 of the '455 patent. {

}

Freescale asserts that the accused products include resistor termination products (Group I) ("Zoran Resistor Termination Products") and hybrid termination products (Groups II and III) ("Zoran Hybrid Termination Products"). (Citing RX-219C at Q. 23-24, 29; RX-218C at Q. 80-98; CX-91C; CX-93C at Nos. 1, 2 and 4.) According to Freescale, both are packaged integrated circuits that serve as the controller chips in digital televisions. (Citing CX-401C at Q. 179.)

Freescale asserts that all Zoran Resistor Termination Products share the same interface circuitry, and for the purpose of infringement of asserted claims 9 and 10 all can be treated identically. (Citing RX-218C at Q. 90; RX-219C at Q. 49, 79.) According to Freescale, all Zoran Hybrid Termination Products share the same interface circuitry, and for the purpose of infringement of asserted claims 9 and 10 all can be treated identically. (Citing RX-218C at Q. 97; RX-219C at Q. 111.)

Freescale asserts that the Zoran Resistor Termination Products infringe claims 9 and 10 of the '455 patent. According to Freescale, each of the accused Zoran Resistor Termination Products have "a data processor within an integrated circuit package." Freescale asserts that Zoran's expert, Dr. Von Herzen, agrees that the Zoran Resistor Termination Products meet this limitation. (Citing Tr. at 568:18-569:11.)

Freescale asserts that the Zoran Resistor Termination Products have "an execution unit internal to the data processor." According to Freescale, Dr. Von Herzen agrees that the Zoran Resistor Termination Products meet this limitation. (Citing Tr. at 568:24-569:11.)

Freescale asserts that the Zoran Resistor Termination Products have "a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus." (Citing CX-401C at Q. 194-196.) According to Freescale, {

} (Citing Tr. at 568:2-17; CX-401C at Q. 194; CX-179C at ZCO 518-19; CX-180C at ZCO 641-42; CX-181C at ZCO 835-36.)

Freescale contends that the Zoran Resistor Termination Products are configured to communicate through a bidirectional DDR2 data bus. (Citing Tr. at 570:4-18; CX-401C at Q. 194; CX-179C at ZCO 459; CX-180C at ZCO 599; CX-181C at ZCO 769.) According to Freescale, the Zoran Resistor Termination Products have {

} (Citing Tr. at 166:9-167:21; JX-40 at ZCO 2821.) Freescale asserts that {

} (Citing Tr. at 166:9-167:21; CX-181C at ZCO 769; CX-96.) According to Freescale, Zoran data sheets { } (Citing CX-181C at ZCO 778.)

Freescale asserts that the Zoran datasheets describe the memory interface of the Zoran Resistor Termination Products as {

} (Citing CX-181C at ZCO 764; CX-179C at ZCO 454; JX-28C at ZCO 952.) According to Freescale, {

} CX-181C, CX-179C and JX-28C. (Citing CX-181C at ZCO 778; CX-179C at ZCO 467; JX-28C at ZCO 953.) Freescale concludes that the {

}

Freescale asserts that Dr. Von Herzen has opined that the accused Zoran products do not practice this limitation because, in his opinion, claim 9 requires an external bus between the pins and the data processor. (Citing Tr. at 570:19-571:3.) Freescale contends that this assertion is mistaken because the phrase "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus" does not require the presence of an external bus for infringement of claim 9, only that the "plurality of external pins" are provided for the purpose of connecting to such an external bus. (Citing CX-401C at Q. 195-196.) According to Freescale, all of the accused Zoran products meet this limitation under a proper reading of claim 9. (Citing Tr. at 167:3-11, 572:6-574:9.)

Freescale asserts that each of the Zoran Resistor Termination Products includes "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit." According to Freescale, the Zoran Resistor Termination Products have a plurality of bus termination circuits under either Freescale's/Staff's or Respondents' constructions of "bus termination circuit." (Citing CX-401C at Q. 197-198.)

Freescale asserts that the "bus termination circuit" of the Zoran Resistor Termination Products is { } (Citing CX-401C at Q. 197.) According to Freescale, the Zoran Resistor Termination Products {

} (Citing CX-179C at ZCO 475; CX-181C at ZCO 786; CX-181C at ZCO 960.) Freescale contends that the {

} JX-29C at ZCO 1035.

(Citing CX-401C at Q. 197; JX-7C at 17:17-20.) According to Freescale, {

} JX-29C at ZCO 1035. (Citing CX-401C at Q. 197.)

Freescale asserts that {

} JX-29C at ZCO 1038. (Citing CX-401C at Q. 197-98.) According to Freescale, the termination circuitry of the Zoran Resistor Termination Products {

} (Citing CX-401C at Q. 197-98.)

Freescale contends that {

} (Citing JX-29C at ZCO 1042.)

Freescale asserts that {

} (Citing CX-401C at Q. 197-98; Tr. at 596:12-598:16.) Freescale contends that {

} (Citing CX-401C at Q. 197-98; Tr. at 167:22-168:7.)

Freescale asserts that {

}

According to Freescale, the Zoran Resistor Termination Products therefore have a plurality of bus termination circuits, each of which is coupled to an external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit.

Freescale asserts that each of the Zoran Resistor Termination Products has "the plurality of bus termination circuits providing data to or receiving data from the execution unit." According to Freescale, {

} (Citing Tr. at 583:23-584:12.) Freescale contends that David Auld testified that{

} (Citing RX-219C at Q. 53.) According to Freescale, when {

} (Citing CX-401C at Q. 199; Tr. at 172:16-173:25.) Freescale asserts that, as {

} (Citing *id.*)

Freescale asserts that Zoran argues that in the Zoran Resistor Termination Circuits {

}

Freescale asserts that after a year of litigation and a hearing on the merits, Zoran has now abandoned its claim construction position for the limitation "the plurality of bus termination circuits providing data to or receiving data from the execution unit." (Citing ZIB at 5.) According to Freescale, Zoran maintains its non-infringement position based on this limitation despite abandoning the corresponding claim construction. Freescale asserts that Zoran's non-infringement position was premised exclusively on Zoran's proposed construction. (Citing

ZPHB at 39-40; RX-218C at Q. 50, 136-171; Tr. at 577:17-578:6.) Freescale asserts that except for a conclusory answer to a single question, Zoran has never argued non-infringement based on the claim construction it now agrees is correct. (Citing RX-218C at Q. 174.)

Freescale asserts that Zoran's own technical documents that { } According to Freescale, Zoran's focus on the lowest level schematics is misplaced. Freescale asserts that JX-40C (Zoran Resistor Termination Products) and JX-37C (Zoran Hybrid Termination Products) { }

Freescale asserts that Zoran admitted that { } (Citing Tr. at 578:24-580:8.) According to Freescale, Zoran admitted that { } of JX-29C at ZCO 1035 { } (Citing RX-219C at Q. 53, 56.) Freescale asserts that Zoran's expert witness and corporate witness both testified that { } (Citing Tr. at 172:16-173:8, 579:21-580:8.) According to Freescale, that { }

Freescale explains that in CDX-4C.4, the line in red is {

} (Citing JX-29C at 1035, 1038; CX-401C at Q. 199.)

Freescale asserts that {

} According to Freescale, Zoran's corporate witness testified as to this { } JX-40C. (Citing Tr. at 166:9-167:21; JX-40 at ZCO 2821.) Freescale asserts that this claim element was previously found to be met by the Zoran Resistor Termination Products for the same reasons being proffered by Freescale. (Citing JX-55 at 63.)

According to Freescale, the Zoran Resistor Termination Products practice "each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal" and have a "conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal." (Citing CX-401C at Q. 200-01.)

Freescale asserts that each of the bus termination circuits in the Zoran Resistor Termination Products has {

} (Citing CX-401C at Q. 197, 200-201.) Freescale contends that any { } (Citing JX-29C at ZCO 1042, 1046) {

} (Citing CX-401C at Q. 197, 200-201.) According to Freescale, the bus

termination circuit {

} (Citing *id.*)

Freescale asserts that each of the Zoran Resistor Termination Products' control signals "when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus." According to Freescale, when an individual one or more {

} (Citing CX-401C at Q. 197, 202-205; Tr. at 596:12-598:16; JX-29C at ZCO 1042, 1046.) {

} (Citing *id.*)

Freescale asserts that the operation of {

} JX-29C at ZCO 1042. (Citing CX-401C at Q. 204; Tr. at 596:12-598:16.) According to Freescale, {

}

Freescale asserts that {

} JX-29C at ZCO 1046. (Citing CX-401C at Q. 204; Tr. at 596:12-598:16.) According to Freescale, {

} (Citing *id.*) According to Freescale, {

}

Freescale asserts in its reply brief that Zoran's non-infringement positions regarding the "a conductor . . ." limitation are based on Zoran's improperly narrow construction of "a conductor," and therefore fail if Zoran's construction is not adopted. Freescale contends that Zoran's first argument rests on its belief that claim 9 requires {

} According to Freescale, this argument is counter to the plain language of the claim, which does not require {

} Rather, Freescale asserts that the only requirement relating to the termination of the pin on a data bus is that at least one circuit component is coupled to the bus to reduce signal reflection on the bus. (Citing JX-1 at 10:26-52.) According to Freescale, utilizing {

} (Citing CX-401C at Q. 202-05.)

Freescale asserts that Zoran's argument that {

} fails. Freescale contends that this argument can only be made under Zoran's interpretation of claim 9 that permits a single control signal on a single common conductor. According to Freescale, if one does not read that limitation into claim 9, thereby allowing control signals on multiple conductors, then Zoran's argument fails. (Citing CX-401C at Q. 201-205.)

Freescale asserts that Zoran's position that only one control signal is permitted by the claim is simply another way of arguing that only one common conductor can be utilized and fails for the same reasons. According to Freescale, the recitation of "a control signal" in the claim

does not limit the claim to only one control signal, nor does it require that one single control signal perform all of the necessary functions. Freescale asserts {

}

(Citing CX-401C at Q. 201-205.) Freescale contends that the Zoran Resistor Termination Products {

}

under Freescale's plain and ordinary meaning construction. (Citing JX-55 at 63-64.)

Freescale asserts that the Zoran Hybrid Termination Products also infringe claim 9 of the '455 Patent. According to Freescale, each of the Zoran Hybrid Termination Products uses the { } (Citing RX-218C at Q. 97; RX-219C at Q. 111; CX-194C at 1; CX-276C at 1; CX-401C at Q. 211-14; JX-30C; JX-53C.)

Freescale asserts that each of the Zoran Hybrid Termination Products have "a data processor within an integrated circuit package." According to Freescale, Dr. Von Herzen agrees that the Zoran Hybrid Termination Products meet this limitation. (Citing Tr. at 568:18-569:11.)

Freescale asserts that each of the Zoran Hybrid Termination Products have "an execution unit internal to the data processor." According to Freescale, Dr. Von Herzen agrees that the Zoran Hybrid Termination Products meet this limitation. (Citing Tr. at 568:24-569:11.)

Freescale asserts that each of the Zoran Hybrid Termination Products have "a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus." According to Freescale, each of the Zoran Hybrid Termination Products has {

} (Citing Tr. at 568:2-17; CX-178C at ZCO 177-83; JX-31C at ZCO 1852-9; JX-32C at ZCO 1991-6; JX-33C at ZCO 2054-9; JX-34C

at ZCO 2413-23; JX-35C at ZCO 2505-10; JX-36C at ZCO 13585-90; JX-37C at ZCO 2322-27; CX-401C at Q. 219-221, 243-45.) Freescale contends that each of the Zoran Hybrid Termination Products { } (Citing CX-178C at ZCO 105; JX-31C at ZCO 1797, 1816-8; JX-32C at ZCO 1937, 1955-7; JX-33C at ZCO 2007, 2024-6; JX-34C at ZCO 2351; JX-37C at ZCO 2250.) According to Freescale, the Zoran Hybrid Termination Products {

} (Citing Tr. at 169:2-170:4; CX-178C at ZCO 108; JX-31C at ZCO 1816-8; JX-32C at ZCO 1955-7; JX-33C at ZCO 2024-6; JX-35C at ZCO 2478-9; JX-36C at ZCO 13563-4; JX-34C at ZCO 2375; JX-37C at ZCO 2253.) Freescale {

} (Citing CX-401C at Q. 219, 243; Tr. at 175:21-178:1.) Freescale contends that the {

} (Citing CX-401C at Q. 219, 243.)

Freescale asserts that Dr. Von Herzen has opined that the accused Zoran products do not practice this limitation because claim 9 actually requires an external bus between the pins and the data processor. (Citing Tr. at 570:19-571:3.) According to Freescale, this assertion is mistaken because the phrase "the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus" does not require the presence of an external bus for infringement of claim 9, only that the "plurality of external pins" are provided for the purpose of connecting to such an external bus. (Citing CX-401C at Q. 220-221, 245.) According to Freescale, all of the accused Zoran Hybrid Termination Products meet this

limitation under a proper reading of claim 9. (Citing CX-401C at Q. 220-221, 245; Tr. at 168:15-170:4, 572:6-574:9.)

Freescale asserts in its reply brief that Zoran dedicates nine lines of its brief to its argument that claim 9 requires an external bus in order to be infringed. According to Freescale, claim 9 merely requires that the plurality of external pins be capable of bidirectionally communicating logic bits to and from the data processor via an external bus. Freescale asserts that there is no structural requirement that the external bus be present in order to meet this claim limitation. (Citing CX-401C at Q. 195-196.) According to Freescale, the Federal Circuit has stated that "apparatus claims cover what a device is, not what a device does." (Citing *Hewlett-Packard v. Bausch & Lomb*, 909 F.2d 1464, 1468 (Fed. Cir. 1990).)

Freescale contends that the preamble of the claim recites "a data processor within an integrated circuit package." (Citing JX-1 at 10:26-27.) According to Freescale, the notion that an external bus is required to infringe a claim directed to a data processor within an integrated circuit package is completely misplaced. Freescale asserts that all of the Zoran products (Resistor and Hybrid) are {

} (Citing Tr. at 167:3-11.) According to Freescale, {

} (Citing Tr. at 572:6-574:9.)

Freescale asserts that each of the Zoran Hybrid Termination Products includes "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit." According to Freescale, the Zoran Hybrid Termination Products have a plurality of bus termination circuits under either Freescale's/Staff's or Respondents'

constructions of the "bus termination circuit" limitation. (Citing CX-401C at Q. 222-223, 246-47.)

Freescale asserts that the relevant portions of the { } JX-30C and JX-53C. According to Freescale, { } JX-30C at ZCO 1047 and JX-53C at ZCO 1269. (Citing CX-401C at Q. 246-47.) Freescale asserts that within { } (Citing JX-7C at 68:20-69:5.) According to Freescale, { } is a "bus termination circuit" under either proposed construction for this term. (Citing CX-401C at Q. 222, 246.) Freescale contends that each instance of { } (Citing Tr. at 175:21-176:12, 596:12-598:16; JX-7C at 67:20-68:5.) Freescale asserts that { } (Citing CX-401C at Q. 222, 246; Tr. at 167:22-168:14.)

Freescale asserts that each of the plurality of { } bus termination circuits in the Zoran Hybrid Termination Products { } (Citing CX-401C at Q. 222, 246; JX-30C at ZCO 1048; JX-53C at ZCO 1272.) Freescale contends that { } (Citing *id.*; Tr. at 180:15-183:10; JX-7C at 71:12-72:8, 74:13-76:13.) Freescale asserts that when

{

} (Citing CX-401C at Q. 222, 246.)

Freescale asserts that under the Respondents' proposed construction, in addition to

{

} (Citing *id.*; JX-7C at 73:8-24, 76:18-78:9.) Freescale asserts that because {

} they meet the Respondents' proposed construction for "bus termination circuit." (Citing CX-401C at Q. 222-23, 246.)

Freescale asserts that the Zoran Hybrid Termination Products further meet the "the plurality of bus termination circuits providing data to or receiving data from the execution unit" limitation, because {

} (Citing Tr. at 175:21-178:1; JX-7C at 71:24-72:8; CX-401C at Q. 224.)

Freescale contends that CDX-4C.11 and CDX-4C.18 show{

} (Citing CX-401C at Q. 224, 248.)

Freescale explains {

} (Citing *id.*) According to Freescale, {

}

(Citing *id.*) As a result, Freescale concludes that the Zoran Hybrid Termination Products have "the plurality of bus termination circuits providing data to or receiving data from the execution unit."

In its reply brief, Freescale asserts that Zoran makes the same arguments for non-infringement of the Zoran Hybrid Termination Products based on this limitation as it did for the Zoran Resistor Termination Products, which Freescale contends fail for the same reasons.

Freescale asserts that {

} (Citing JX-30C at 1047, 1048.) According to Freescale, {

} (Citing Tr. at 175:21-178:1.)

Freescale further asserts that the bus termination circuitry of the Zoran Hybrid Termination Products is found within the { } (Citing Tr. at 169:24-170-4.) Freescale contends that {

} (Citing Tr. at 169:2-170:4; JX-37C at ZCO 2176.)

Freescale asserts that the Zoran Hybrid Termination Products meet the limitation "each bus termination circuit in the plurality of bus termination circuits having an input for receiving a

control signal." (Citing CX-401C at Q. 225, 249; Tr. at 180:15-181:4.) Freescale contends that {

} (Citing JX-30C at ZCO 1047; JX-53C at ZCO 1269.) According to Freescale, the bus termination circuit {

}

(Citing *id.*)

Freescale asserts that each of the Zoran Hybrid Termination Products have "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus." According to Freescale, {

} (Citing CX-401C at Q. 227, 251.) Freescale asserts that these {

} DQ { }

(Citing Tr. at 180:15-183:10; JX-30C at ZCO 1048.) According to Freescale, when {

} (Citing *id.*)

Freescale asserts that the termination circuitry in the bus termination circuit {

} (Citing JX-30C at ZCO 1048; JX-53C at ZCO 1272; JX-7C at 68:20-69:5.) According to Freescale, {

} (Citing JX-7 at 76:18-78:9.) Freescale contends that this is demonstrated in CDX-4C.13 and CDX-4C.20, which are annotated {

}

circuits in the lower red box. (Citing CX-401C at Q. 227-28; JX-30C at ZCO 1048; JX-53C at ZCO 1272.)

Freescale asserts that {

} (Citing JX-30C at ZCO 1048; JX-53C at ZCO 1272; CX-401C at Q. 229, 253.) According to Freescale, {

} (Citing *id.*) Freescale contends that when the {

} (Citing *id.*)

According to Freescale, when the {

} (Citing *id.*)

Freescale asserts that {

} (Citing JX-

30C at ZCO 1048; JX-53C at ZCO 1272; CX-401C at Q. 230, 254.) According to Freescale, the { } (Citing *id.*) According to Freescale, { } (Citing *id.*; JX-7C at 76:18-78:9.)

Freescale contends that Zoran additionally argues that { } According to Freescale, this argument fails in light of long-standing patent law that states infringement is not avoided when an accused device has elements or functionality in addition to those specifically claimed. (Citing *Vulcan Engineering Co., Inc. v. Fata Aluminum, Inc.*, 278 F.3d 1366, 1375 (Fed.Cir.2002); *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 945 (Fed.Cir.1990).)

Freescale asserts that Zoran argues that {

} (Citing CX-401C at Q. 222, 246.) Freescale asserts that the {

} (Citing Tr. at 181:5-182:8.)

Freescale asserts that each of the Zoran Resistor Termination Products infringe claim 10 of the '455 patent. According to Freescale, the Zoran Resistor Termination Products practice the claim 10 limitation that requires that "at least one circuit component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, an electrical short circuit, and an inductor." Freescale asserts that the {

} (Citing CX-401C at Q. 207-09; Tr. at 596:12-598:16.)

Freescale asserts that each of the Zoran Hybrid Termination Products infringe claim 10 of the '455 patent. According to Freescale, the Zoran Hybrid Termination Products practice the claim 10 limitation that requires that "at least one circuit component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, an electrical short circuit, and an inductor." According to Freescale {

} (Citing CX-401C at Q. 231-35, 256-59; Tr. at 599:19-602:7.)

Zoran's Position: Zoran asserts that the Accused Zoran Products do not infringe claims 9 and 10 of the '455 Patent. Zoran agrees with Freescale that that the Accused Zoran Products fall into two groups: resistor termination products and hybrid termination products. Zoran agrees with Freescale regarding the identification of accused Zoran Resistor Termination Products. Zoran asserts that the representative schematics that Zoran's and Freescale's respective experts used to analyze the Zoran Resistor Termination Products is JX-29C. (Citing RX-218C at Q. 89; CX-401C at Q. 197-205.) Zoran asserts that these schematics are representative of the Zoran Resistor Termination Products. (Citing Tr. at 163:17-164:5.) According to Zoran, the Zoran Resistor Termination Products all {

} (Citing RX-218C at Q. 80-81, 84, 88; RX-219C at Q. 48-49, 79-81; Tr. at 284:13-285:1.) Zoran asserts that there are {

} in the different Zoran Resistor Termination Products. (Citing RX-218C at Q. 84.)

Zoran agrees with Freescale regarding the identification of the accused Zoran Hybrid Termination Products. Zoran asserts that the Zoran Hybrid Termination Products have {

} (Citing RX-218C at Q. 93, 239; RX-219C at Q. 21, 107; Tr. at 178:16-24.) According to Zoran, the hybrid circuits in all of the Zoran Hybrid Termination Products are the same. (Citing RX-218C at Q. 97.) Zoran asserts that the representative sets of schematics that Zoran's and Complainant's respective experts used

to analyze this set of products are JX-30C and JX-53C. (Citing RX-218C at Q. 96-97; CX-401C at Q. 222-230, 249-254; Tr. at 165:7-14.)

Zoran asserts that the Zoran Resistor Termination Products do not have "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus." According to Zoran, the Zoran Resistor Termination Products have {

} (Citing Tr. at 586:21-587:8, 592:23-594:2; RX-218C at Q. 162-170, 191; RX-219C at Q. 56, 60-65; JX-29C at ZCO00001038, 1042, 1046; RDX-10-6C; RDX-10-7C.) According to Zoran, the "bus termination circuit" in the accused Zoran products comprises the combination of {

} (Citing Tr. at 586:21-587:8, 593:5-594:2.)

Zoran explains that {

} (Citing JX-29C at ZCO00001038; RX-218C at Q. 164, 193, 195; RX-219C at Q. 60, 73; Tr. at 309:24-310:8, 310:17-311:4; RDX-10-8C.) Zoran explains that each of

the {

} (Citing JX-29C at ZCO00001038, 1043; RX-218C at Q. 192-195, 197; RX-219C at Q. 70-73, 76-78; Tr. at 310:17-311:11; RDX-10-8C; RDX-10-9C.)

Zoran asserts that the {

} (Citing JX-29C at ZCO00001046; RX-218C at Q. 196-197; RX-219C at Q. 75-77; RDX-10-10C.) Zoran explains that the {

} (Citing JX-29C at ZCO00001046; RX-218C at Q. 197; RX-219C at Q. 76; Tr. at 311:23-312:14, 312:20-314:6.)

Zoran explains that RDX-10-11C is an annotated excerpt of the bottom of the { } in RDX-10-10C. (Citing RX-218C at Q. 198; JX-29C at ZCO00001046.) According to Zoran, RDX-10-11C shows that the {

} (Citing RX-218C at Q. 199-200; RX-219C at Q. 77; JX-29C at ZCO00001046.) Zoran contends that the {

} (Citing Tr. at 307:23-309:23, 314:7-24 (Dr. Subramanian); JX-29C at ZCO00001039, 1042; RDX-10-6C; RX-218C at Q. 191; RX-219C at Q. 69.)

Zoran asserts that the Zoran Resistor Termination Products do not infringe claim 9 under Respondents' construction of "a conductor." First, Zoran asserts that Freescale does not contend that any Zoran product infringes claim 9 under Respondents' or Staff's proposed construction of "a conductor." (Citing Tr. at 303:3-304:2.) Second Zoran asserts that each bus termination circuit in the Zoran Resistor Termination Products consists of a {

}

Zoran asserts that this claim limitation expressly requires that the assertion and deassertion of "the control signal" on the conductor "allows each bus termination circuit in the plurality of bus termination circuits" to couple and decouple a circuit component to the bus. (Citing JX-1 at 10:44-52; Tr. at 316:1-7.) Zoran contends that in Zoran Resistor Termination

Products, as Freescale's expert admitted, {

} (Citing Tr. at 316:8-12, 316:20-317:14.) Zoran asserts that, contrary to the claim which requires that the claimed conductor be "coupled to each input of each of the bus termination circuits," {

}

Zoran asserts that even if Freescale's construction of "a conductor" were correct and the claim permits the use of multiple conductors, the remainder of the claim language that provides "coupled to each input of each of the bus termination circuits" and "the control signal . . . allows each bus termination circuit in the plurality of bus termination circuits to couple . . ." expressly requires that all of any such multiple conductors (whether it be one, two or more conductors) be coupled to "each" input of "each" of the bus termination circuits, and that there be a control signal capable of allowing "each" of the termination circuits to couple and decouple a circuit component to the bus. (Citing JX-1 at 10:42-52.) Zoran contends the accused Zoran Resistor Termination Products are not configured in such a way.

In its reply brief, Zoran asserts that Freescale concedes that the bus termination circuits in the Resistor Termination Circuit Products {

} (Citing CIB at 38-41.) According to Zoran, the Zoran Resistor Termination Products lack the limitation requiring "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus

termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus" as a result.

Zoran asserts that the Zoran Resistor Termination Products also do not practice the claim 9 limitation that requires "the plurality of bus termination circuits providing data to or receiving data from the execution unit." (Citing JX-1 at 10:37-39.) Zoran asserts that the schematics for the Zoran Resistor Termination Products {

} (Citing RX-218C at Q. 159; RX-219C at Q. 42-49.) According to Zoran, RDX-10-4C is an annotated copy of the detailed portion of the { } within the Resistor Termination Circuit Products. (Citing JX-29C at ZCO00001035; RX-218C at Q. 160; RX-219C at Q. 48, 53.) Zoran explains that the {

} (Citing JX-29C at ZCO00001035; RX-218C at Q. 161; RX-219C at Q. 53; Tr. at 172:16-173:23, 291:18-24, 296:13-15, 295:18-23; RDX-10-4C.)

Zoran asserts that the {

} (Citing RDX-10-4C; JX-29C at ZCO00001035; RX-218C at Q. 161; RX-219C at Q. 53; Tr. at 174:2-175:9, 291:14-17, 291:25-292:3.)

Zoran asserts that the {

} (Citing RDX-10-4C; JX-29C at ZCO00001035; RX-218C at Q. 161, 172; RX-219C at Q. 53-60; Tr. at 290:21-291:8.) Zoran explains that {

}

(Citing Tr. at 292:4-12, 293:5-15, 294:14-23, 602:20-603:16.) Zoran contends that {

} (Citing Tr. at 293:16-23.) Zoran concludes that, as a result, the bus termination circuits do not, as the claim requires, receive data from the execution unit. (Citing RX-218C at Q. 174; Tr. at 174:2-175:9.)

Zoran asserts that the bus termination circuits {

} (Citing RX-218C at Q. 173.) According to Zoran, {

} (Citing Tr. at 172:16-173:23, 290:8-20, 295:18-23, 296:13-15; JX-29C at ZCO00001035; RX-161C at Q. 161; RDX-10-4C.) Zoran asserts that Dr. Subramanian admitted that the {

} (Citing Tr. at 296:24-297:8.) According to Zoran, Dr. Subramanian further acknowledged that {

} (Citing Tr. at 296:16-23.)

Zoran asserts that the lower level schematics that depict {

} (Citing JX-29C at ZCO00001038; RX-218C at Q. 162-163.) Zoran explains that the {

} (Citing RX-218C at Q. 164; RX-219C at Q. 56, 60; Tr. at 586:21-587:8.)

Zoran asserts that annotated copies of the schematics from JX-29C {

} (Citing RX-218C at Q. 170-171; RX-219C at Q. 67-68; JX-29C at ZCO00001042, 1046.) According to Zoran, {

} (Citing RX-218C at Q. 170-171; RX-219C at Q. 67-68.) Zoran concludes, as a result, that the schematics confirm that the bus termination circuits do not provide data to or receive data from the execution unit as required by claim 9. (Citing RX-218C at Q. 174, 136-137.)

Zoran asserts that Dr. Subramanian relies on the {

} (Citing RX-218C at Q. 170-171, 177-178; RX-219C at Q. 67-68; JX-29C at ZCO00001035, 1038, 1042, 1046.)

Zoran asserts that Dr. Subramanian opines that {

} According to Zoran, this it is a conclusion by an expert that is unsupported by any evidence or analysis and, as such, must be rejected. (Citing *Yoon Ja Kim v. ConAgra Foods, Inc.*, 465 F.3d 1312, 1320 (Fed. Cir. 2006); *Certain Elec. Imaging Devices*, Inv. No. 337-TA-726, Final Init. Det. at 45 (July 27, 2011).) Zoran asserts that there is no evidence that the {

}

In its reply brief, Zoran contends that Freescale does not contend that the {

}

(Citing CIB at 38.) According to Zoran, Freescale's contention is limited to asserting that {

} (Citing CIB at 38.) Zoran asserts that this contention is incorrect.

Zoran asserts that the schematics for the Resistor Termination Products establish that {

}

Zoran asserts that Freescale attempts to circumvent these facts by {

} (Citing *id.* at Q. 203; CDX-4C.6.)

Zoran asserts that Freescale's post-hearing brief cites the hearing testimony of Mr. Auld and Dr. Von Herzen in purported support for its { } (Citing CIB at 37-38.) According to Zoran, the cited Auld testimony does not mention the { } (Citing Tr. at 172:16-173:25.) Zoran asserts that the cited Von Herzen testimony also does not state or suggest that the { } (Citing Tr. at 583:23-584:12, 596:12-598:16.) According to Zoran, Dr. Von Herzen's testimony is that the {

} (Citing Tr. at 583:23-584:12.)

Zoran asserts that the Zoran Hybrid Termination Products do not infringe claim 9 of the '455 patent. Zoran asserts that RDX-10-14C is an annotated copy of the { } of the Zoran Hybrid Termination Products. (Citing JX-30C at ZCO00001048; RX-218C at Q. 247-248; RX-219C at Q. 100-101.) According to Zoran, the Zoran Hybrid Termination Products have { } (Citing Tr. at 178:16-180:8, 194:18-195:23, 599:25-600:24, 601:23-602:7; JX-30C at ZCO00001048; RX-218C at Q. 237-238, 249; RDX-10-13C.) Zoran explains that RDX-10-14C shows the {

}

Zoran asserts that the {

} (Citing JX-30C at ZCO00001048; RX-218C at Q. 249-250; RX-219C at Q. 100-104; Tr. at 197:22-199:9, 317:23-319:12, 320:2-18, 599:25-602:7; RDX-10-14C; JX-53C at ZCO00001272.) According to Zoran, the {

} (Citing JX-53C at ZCO00001272; Tr. at 319:13-320:1, 320:19-321:6.)

Zoran asserts that the schematics for the Zoran Hybrid Termination Products {

} (Citing *id.*)

Zoran asserts that the Zoran Hybrid Termination Products do not have "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to

decouple at least one circuit component from the bus." According to Zoran, Freescale does not contend that the Zoran Hybrid Termination Products infringe claim 9 under Respondents' or Staff's proposed construction of this claim limitation; each of the plurality of Zoran bus termination circuits {

}

Zoran asserts that Freescale's infringement claim fails for the additional reason that Complainant incorrectly identifies the {

} (Citing CX-401C at Q. 222; JX-30C at ZCO00001047-1048.) Zoran contends that the {

} (Citing JX-30C at ZCO00001047-1048; RX-218C at Q. 93, 236, 239; RX-219C at Q. 21, 99, 107; Tr. at 178:16-24, 300:7-10, 599:19-24.)

Zoran asserts that the {

} in the Zoran Hybrid

Termination Products. (Citing JX-30C at ZCO00001048; RX-218C at Q. 249; RX-219C at Q103-104; RDX-10-14C; JX-53C at ZCO00001272; Tr. at 318:17-319:21, 320:2-25.) Zoran asserts that {

} (Citing JX-30C at ZCO00001048; RDX-10-14C; RX-218C at Q. 249; RX-219C at Q. 104.) Zoran asserts that the {

} (Citing Tr. at 318:17-319:21, 320:2-25; RX-218C at Q. 249; RX-219C at Q. 104.)

Zoran asserts that the collection of the {

} (Citing JX-30C at ZCO00001048; Tr. at 197:12-21, 321:7-322:12.) {

} (Citing Tr. at 181:5-19, 181:24-182:4, 196:7-197:11.) According to Zoran, the {

} (Citing Tr. at 182:16-183:4, 196:7-197:11.)

Accordingly, Zoran asserts that there is no basis to Freescale's contention that {

} satisfy the requirements of claim 9.

Zoran asserts in its reply brief that Freescale's post-trial brief does not contend that the Zoran Hybrid Termination Products infringe claim 9 under Respondents' or Staff's proposed construction of this claim limitation. Zoran further asserts that Freescale's infringement theory fails under either party's view of the proper construction of the "a conductor" element of this claim limitation. Zoran contends that Freescale identified {

}

Zoran contends that the circuitry within the {

.}

Zoran asserts that the Zoran Hybrid Termination Products also lack the claimed "plurality of bus termination circuits providing data to or receiving data from the execution unit." (Citing RX-218C at Q. 232-233.) According to Zoran, the schematics for the Zoran Hybrid Termination Products {

} (Citing RX-218C at Q. 234; RX-219C at Q. 91-98; JX-30C at ZCO00001047.)

Zoran asserts that RDX-10-12C is an annotated copy of the detailed portion of the {

} within the Hybrid Termination Circuit Products. (Citing JX-

30C at ZCO00001047; RX-218C at Q. 235.) Zoran explains that the {

} (Citing JX-30C at ZCO00001047; RX-218C at Q. 236; RX-219C at Q. 99; Tr. at 176:3-177:8, 299:9-22, 300:7-10; RDX-10-12C.) Zoran explains that the {

} (Citing JX-30C at ZCO00001047; RX-218C at Q. 236; RX-219C at Q. 99; Tr. at 177:9-178:1, 299:23-300:6.)

Zoran asserts that {

} (Citing Tr. at 603:17-605:16.)

Zoran contends that the {

} (Citing RX-218C at Q.

237-239; RX-219C at Q. 107; JX-30C at ZCO00001048; RDX-10-13C.) {

} (Citing Tr. at 176:3-177:8, 300:7-10.)

Zoran asserts that {

} (Citing RX-219C at Q. 107; RX-218C at Q. 239; JX-30C at ZCO00001047-1048; Tr. at 302:10-18.) {

}

(Citing RX-219C at Q. 106; RX-218C at Q. 239-240, 232-233.)

Zoran asserts that Dr. Subramanian points to {

} (Citing RX-218C at Q. 239; RX-219C at Q. 106-107; JX-30C at ZCO00001047, ZCO00001048; RDX-10-12C; RDX-10-13C.) {

} (Citing CX-401C at Q. 224, 228.)

According to Zoran, this argument should be rejected for the same reasons as Dr. Subramanian's argument regarding the Zoran Resistor Termination Products.

Zoran asserts in its reply brief that the argument that Freescale makes in its post-trial brief as to the presence of this claim limitation in the Zoran Hybrid Termination Products is premised upon its {

} (Citing CIB at 46-47.) Zoran asserts that the {

} (Citing JX-1 at 10:37-39.)

Zoran asserts that {

}

Zoran asserts that neither the Zoran Resistor Termination Products nor the Zoran Hybrid Termination Products includes "a plurality of external pins connected to the integrated circuit package, the plurality of pins used to bidirectionally communicate logic bits to and from the data processor via an external bus." Zoran notes that claim 9 is an apparatus claim, one element of

which requires an "external bus." (Citing JX-1 at 10:26-27, 10:31-32.) {

} (Citing RX-218C at Q. 113-114, 124, 221, 225; Tr. at 193:1-12, 286:9-18.) {

} (Citing RX-218C at Q. 113-114, 221; Tr. at 570:19-571:3.) According to Zoran, Dr. Subramanian conceded that if the recited "an external bus" is a claim limitation, then Zoran's products do not infringe claim 9. (Citing Tr. at 286:19-287:6.)

Zoran asserts that Freescale argues that the recited "external bus" apparatus is not required by this apparatus claim, and that, instead, the apparatus requirements imposed by this claim limitation stop with the words "plurality of external pins," with the following sixteen words of the limitation merely stating the "purpose" of the pins. (Citing CIB at 36, 44.) Zoran disagrees and asserts that the language of the claims and intrinsic evidence do not support such a reading. According to Zoran, Freescale identifies no intrinsic support for its position.

Zoran asserts that the accused Zoran ICs do not infringe asserted claims 9 or 10 of the '455 patent under the doctrine of equivalents and Freescale has introduced no evidence of such infringement. (Citing Tr. at 285:11-16; RX-218C at Q. 127-128, 175-176, 201, 228-229, 241-242, 251.)

Zoran asserts that the accused Zoran ICs do not infringe asserted claims 9 or 10 of the '455 patent indirectly and Freescale has introduced no evidence of such infringement. (Citing Tr. at 285:17-22.)

Staff's Position: Staff asserts that the accused Zoran ICs do not meet the "a conductor . . ." limitation of claim 9. According to Staff, Dr. Subramanian identifies multiple control *signals* and multiple conductors as satisfying the "a conductor" limitation. Staff asserts, however, that

{

} (Citing RX-218 at Q. 197, 200, 249-50; Tr. at 308:22-309:23, 311:2-312:14, 316:19-317:14, 318:8-321:6.)

Staff asserts that, alternatively, the evidence of record demonstrates that {

} (Citing Tr. at 179:11-180:8, 181.12-182:2, 195:4-11, 305:21-306:4, 587:1-18.) Staff asserts that Dr. Subramanian's opinion that {

} Staff contends that Dr. Von Herzen testified that { } (Citing Tr. at 593:13-594:2.) Staff concludes that at a minimum, at {

}

Staff disagrees with Freescale's contention {

}

(Citing CX-401C at Q. 222; JX-30C at ZCO00001047-1048.) Staff asserts that {

} (Citing JX-30C at ZCO00001047-1048; RX-218C at Q. 93, 236, 239; RX-219C at Q. 21, 99, 107; Tr. at

178:16-24, 300:7-10, 599:19-24.) According to Staff, {

} (Citing JX-30C at ZCO00001048; RX-218C at Q. 249; RX-219C at Q. 103-104; RDX-10-14C; JX- 53C at ZCO00001272; Tr. at 318:17-319:21, 320:2-25.)

Staff asserts {

} (Citing JX-1 at Figures 1-2, 5, 6-8.)

Discussion and Conclusions: Based on the evidence in the record, I find that Freescale has proven by a preponderance of the evidence that the Accused Zoran Resistor Termination Products infringe asserted claims 9 and 10 of the '455 patent; but Freescale has failed to prove by a preponderance of the evidence that the Accused Zoran Hybrid Termination Products meet the claim 9 limitation that requires that "wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit

component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus."

Zoran and Freescale agree that the Zoran Resistor Termination Products {

} share the same interface circuitry and for the purposes of infringement of claims 9 and 10 can be treated the same. (CIB at 33; ZIB at 6-7.) As discussed in Section V *supra*, Freescale's infringement allegations directed to ZR39770BGCF, ZR39772HGCF-B, ZR39775HGCF-B, ZR39775HGCF-TC, ZR39775HGCF-TC-LP, ZR39785HGCF-B, ZR39787HGCF, and ZR39787HGCF-LP are precluded. As a result, the only Zoran resistor termination products relevant for purposes of infringement are {

} (collectively "the Accused Zoran Resistor Termination Products"). Because Zoran and Freescale agree that the Accused Zoran Resistor Termination Products can be treated the same for purposes of infringement of claims 9 and 10, they will be treated identically as a group.

Zoran and Freescale agree that the Zoran Hybrid Termination Products {

} share the same interface circuitry and for the purposes of infringement of claims 9 and 10 can be treated the same. (CIB at 33; ZIB at 6-7.)

Zoran and Freescale entered into a stipulation as to the Zoran products actually imported,

but that stipulation does not include ZR39501HGCG, ZR39504HGCG, and ZR39505HGCG. (*See* CX-274C; CIB at 97-98.) Freescale's only argument regarding importation of these three products was based on the fact that any exclusion order covering the products included in the stipulation would also cover these three products. (*See* CIB at 97-98.) This argument fails to address the question of *importation* of ZR39501HGCG, ZR39504HGCG, and ZR39505HGCG. Because Freescale failed to introduce any evidence that ZR39501HGCG, ZR39504HGCG, and ZR39505HGCG were imported, the only Zoran hybrid termination products relevant for purposes of infringement are {

} (collectively "the Accused Zoran Hybrid Termination Products"). Because Zoran and Freescale agree that the Accused Zoran Hybrid Termination Products can be treated the same for purposes of infringement of claims 9 and 10, they will be treated identically as a group.

Accused Zoran Resistor Termination Products

The dispute between Freescale and Zoran focuses on four separate parts of claim 9: (1) an external bus, (2) a plurality of bus termination circuits, (3) the plurality of bus termination circuits providing data to or receiving data from the execution unit, and (4) a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least

one circuit component from the bus. As explained below, Zoran's non-infringement arguments based on these elements are not persuasive.

The first dispute between Freescale and Zoran focuses on the limitation that requires "a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus." The evidence shows that the Accused Zoran Resistor Termination Products have a plurality of external pins connected to the integrated circuit package. (CX-401C at Q. 194; Tr. at 568:7-17.) The evidence also shows that these plurality of external pins are ***used*** to bidirectionally communicate logic bits to and from the data processor via an external bus. (CX-401C at Q. 194; Tr. at 569:12-570:18.) The only dispute between is whether or not this claim limitation requires the actual presence of an "external bus" within the accused product to be infringed. (*See* Tr. at 570:19-571:3.) It does not.

Zoran's arguments that an external bus is required by this claim limitation are not persuasive. Claim 9 is an apparatus claim. (JX-1 at 10:26-27.) "[A]pparatus claims cover what a device is, not what a device does." *Hewlett-Packard v. Bausch & Lomb*, 909 F.2d 1464, 1468 (Fed. Cir. 1990); *Certain Liquid Crystal Display Devices, Including Monitors, Televisions, and Modules, and Components Thereof*, Inv. Nos. 337-TA-749, 337-TA-741, Initial Determination (January 12, 2012) ("*Liquid Crystal Display Devices*"). In *Liquid Crystal Display Devices*, I addressed whether or not an apparatus that performed certain actions when it received an input video signal required the presence of the input video signal to be infringed. I found that the accused apparatus did not need to include the input video signal within the accused device to infringe. Rather, it only needed to perform certain actions if presented with an input video signal.

Similar facts present themselves here—claim 9 requires "a plurality of external pins connected to the integrated circuit package, the plurality of external pins ***used*** to bidirectionally communicate logic bits to and from the data processor via an external bus." The claim language "the plurality of external pins ***used*** to bidirectionally communicate logic bits to and from the data processor via an external bus" states what the plurality of external pins *are used to do*, not what the device *is*.[9] As a result, like the "input video signal," the "external bus" need not be present in the accused device itself to find infringement. Because the presence of an "external bus" is not required in the accused device itself, Freescale has proven by a preponderance of the evidence that the Accused Zoran Resistor Termination Products have "a plurality of external pins connected to the integrated circuit package, the plurality of external pins used to bidirectionally communicate logic bits to and from the data processor via an external bus."

The second dispute between Freescale and Zoran is whether or not the Accused Zoran Resistor Termination Products have "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit." The preponderance of the evidence shows that the Accused Zoran Resistor Termination Products meet this limitation.

The Accused Zoran Resistor Termination Products have "a plurality of bus termination circuits" under the parties' agreed construction. JX-29C[10] at ZCO 1038 depicts three instances

{

} (JX-29C at ZCO 1038.) {

---

[9] Zoran's expert admitted that the "plurality of external pins" in the Zoran Resistor Termination Products can be used to bidirectionally communicate logic bits to and from the data processor via an external bus. (Tr. at 569:12-570:18.)

[10] Zoran admits that JX-29C is a representative set of schematics for the circuitry contained in the Accused Zoran Resistor Termination Products. (Tr. at 163:17-164:5; ZIB at 6.)

} (JX-29C at ZCO 1042, 1046; RX-219C at Q. 59-60.) {

} "circuitry for signal termination that is selectively enabled or disabled in response to [a] control signal whose assertion is based, at least in part, on the direction of data signals on the bus."

The Accused Zoran Resistor Termination Products also have "one bus termination circuit being coupled to one external pin of the plurality of external pins." JX-29C at ZCO 1038 depicts {

} (RX-219C at Q. 53; Tr. at 165:15-168:7, 583:13-18.) Thus, the accused bus termination circuits are coupled to an external pin of the plurality of external pins.

The Accused Zoran Resistor Termination Products also meet the limitation requiring that "wherein each external pin is coupled to at least one bus termination circuit." Zoran admits that

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} (Tr. at 165:15-168:7.) {

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As a result, Freescale has proven by a preponderance of the evidence that the Accused Zoran Resistor Termination Products have "a plurality of bus termination circuits, one bus termination circuit being coupled to one external pin of the plurality of external pins wherein each external pin is coupled to at least one bus termination circuit."

The third dispute between Freescale and Zoran is whether or not the Accused Zoran Resistor Termination Products have "the plurality of bus termination circuits providing data to or receiving data from the execution unit." The preponderance of the evidence shows that the Accused Zoran Resistor Termination Products meet this limitation.

Zoran admits that when data is received by the Accused Zoran Resistor Termination Products, {

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This finding is consistent with the specification of the '455 patent. Figures 2, 6, and 7 of the '455 patent depict bus termination circuits connected in parallel with the data bus. (*See* JX-1

at Figs. 2, 6, 7.) Like the accused products, in Figures 2, 6, and 7 the bus termination circuits ("Termination Circuit/Component") connect between the data bus and ground or VDD, but the data signal does not pass *through* the resistor components of the bus termination circuits when being transmitted between the external pin and the execution unit. (*See* JX-1 at Figs. 2, 6, 7.) Dr. Von Herzen admitted that, although not identical, the structure in Figure 2 of the '455 patent parallels the structure of the Accused Zoran Resistor Termination Products. (Tr. at 591:18-592:2.) Although, the specification of the '455 patent does depict one embodiment in Figure 8 showing the bus termination circuits connected in series with the data bus (JX-1 at Fig. 8), there is no language identified by Zoran in claim 9 indicating that claim 9 should be limited to this single embodiment. Moreover, a construction that excludes a preferred embodiment (such as shown in Figures 2, 6, and 7) is rarely, if ever, correct. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) (citing *Modine Mfg. Co. v. United States Int'l Trade Comm'n*, 75 F.3d 1545, 1550, 37 USPQ2d 1609, 1612 (Fed.Cir.1996)).[11]

Zoran's arguments also fail because Zoran waived any non-infringement arguments under a plain and ordinary meaning of this limitation by failing to address them in its pre-hearing brief. Zoran's pre-hearing brief did not assert that this claim term was not met by the Accused Zoran Resistor Termination Products under a plain and ordinary meaning. (*See* ZPHB at 39-45.) Rather, Zoran's only argument that this limitation was not met turned on its construction that "requires that the bus termination circuits actually provide data to and receive data from the execution unit." (ZPHB at 39.) As provided by Ground Rule 8.2, "[a]ny contentions not set forth in detail as required herein shall be deemed abandoned or withdrawn, except for

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[11] Zoran waived any argument that claim 9 should be construed to be limited to the embodiment shown in Figure 8 when it withdrew its proposed claim construction for this limitation and agreed to "plain and ordinary meaning" in its post-hearing brief. (See ZIB at 18-19; ZPHB at 26-32.)

contentions of which a party is not aware and could not be aware in the exercise of reasonable diligence at the time of filing the pre-trial brief." Because Zoran failed to set forth this non-infringement defense under a plain and ordinary meaning of this claim limitation in its prehearing brief, this argument was waived.[12]

The fourth dispute between Freescale and Zoran is whether or not the Accused Zoran Resistor Termination Products have "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus." Freescale has shown by a preponderance of the evidence that the Accused Zoran Resistor Termination products meet this limitation.

JX-29C at 1038 {

} (Tr. at 592:23-598:16.)

[12] This waiver does not change Freescale's burden to prove infringement by a preponderance of the evidence.

Zoran's non-infringement arguments based on this limitation (even those purportedly under Freescale's construction of "a conductor") all appear to stem from Zoran's reading of claim 9 to require that a conductor connected to one bus termination circuit must also be connected to *all* other bus termination circuits and any control signals provided on the conductor must cause *all* bus termination circuits to couple or decouple circuit components to the bus. In Section III.B.3 *supra*, I found that "a conductor" is not limited to a single common conductor, but is "one or more conductors." For the same reasons discussed in Section III.B.3, a "control signal" is not properly limited to a single common control signal, but is "one or more control signals." Zoran's related argument that the {

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Ultimately, there is no requirement in the claims that one control signal be provided to all bus termination circuits over a common conductor that couples circuit components to the bus in all bus termination circuits when asserted. (*See* JX-1 at 10:42-52; *see also* Section III.B.3 *supra*.) Claim 9 merely requires (one or more) conductor(s) coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the (one or more) conductor(s) providing (one or more) control signal(s) wherein the (one or more) control signal(s), when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus. The evidence shows that this limitation is met by the Accused Zoran Resistor Termination Products.

Freescale has proven by a preponderance of the evidence that the remaining claim

limitations included in claim 9 are met by the Accused Zoran Resistor Termination Products. First, the Accused Zoran Resistor Termination Products include "a data processor within an integrated circuit package." Zoran does not dispute this limitation was met and Dr. Von Herzen, Zoran's expert, agrees that the Accused Zoran Resistor Termination Products meet this limitation. (Tr. at 568:18-23.) Second, the Accused Zoran Resistor Termination Products have "an execution unit internal to the data processor." Zoran does not dispute this limitation was met, and Dr. Von Herzen, Zoran's expert, agrees that the Accused Zoran Resistor Termination Products meet this limitation. (Tr. at 568:24-569:11.) Third, the Accused Zoran Resistor Termination Products meet the limitation requiring that "each bus termination circuit in the plurality of bus termination circuits having an input for receiving a control signal." As discussed above, {

} (RX-219C at Q.71-77; Tr. at 596:12-598:16.) Thus, in the Accused Zoran Resistor Termination Products, each bus termination circuit has an input for receiving a control signal.

Based on the foregoing, I find that Freescale has proven by a preponderance of the evidence that the Accused Zoran Resistor Termination Products infringe asserted claim 9 of the '455 patent.

Freescale has likewise proven by a preponderance of the evidence that the Accused Zoran Resistor Termination Products infringe asserted claim 10 of the '455 patent because the bus termination circuits include at least one circuit component "wherein the at least one circuit component is a circuit component selected from a group consisting of: a capacitor, a diode, a resistor, a transistor, a voltage source, a current source, an electrical short circuit, and an inductor." (JX-1 at 10:63-57.) JX-29C at ZCO 1042 and 1046 show that the circuit components

within the accused bus termination circuits are resistors. Indeed, Dr. Von Herzen admitted that {

} (Tr. at 592:23-595:7, 596:12-598:7.)

Accused Zoran Hybrid Termination Products

Freescale has failed to meet its burden to show that the Accused Zoran Hybrid Termination Products include "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus." Zoran and Freescale both agree that JX-30C and JX-53C are representative schematics for the Accused Zoran Hybrid Termination Products. (CIB at 44-45; ZIB at 7.) Freescale has asserted {

} (JX-30C at ZCO 1048 and JX-53C at ZCO 1272.)

Freescale relies on testimony from Mr. Auld, a Zoran witness, to attempt to show a link between {

} A plain and ordinary reading of "allows" does not permit such an attenuated relationship between the accused control signal and whether circuitry is coupled to or decoupled from the bus. Moreover, nothing in the intrinsic record supports Freescale's position on this issue. (*See generally* JX-1; JX-2.)

Because Freescale has failed to show anything but an attenuated link between the accused {

} As a result, Freescale has failed to prove by a preponderance of the evidence that the Accused Zoran Hybrid Termination Products include "a conductor coupled to each input of each of the bus termination circuits in the plurality of bus termination circuits, the conductor providing the control signal wherein the control signal, when asserted, allows each bus termination circuit in the plurality of

bus termination circuits to couple at least one circuit component to the bus to reduce signal reflection on the bus, the control signal, when deasserted, allows each bus termination circuit in the plurality of bus termination circuits to decouple at least one circuit component from the bus."

Based on the foregoing, I find that Freescale has failed to prove by a preponderance of the evidence that the Accused Zoran Hybrid Termination Products infringe asserted claim 9 of the '455 patent. Claim 10 depends from claim 9 and incorporates all claim 9 limitations. As a result, for the same reasons discussed above, Freescale has failed to demonstrate by a preponderance of the evidence that the Accused Zoran Hybrid Termination Products infringe asserted claim 10 of the '455 patent. *Wahpeton Canvas Co. v. Frontier, Inc.*, 870 F.2d 1546, 1552 n. 9 (Fed. Cir. 1989) ("One who does not infringe an independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim.")

VII. DOMESTIC INDUSTRY

A. Applicable Law

In patent-based proceedings under section 337, a complainant must establish that an industry "relating to the articles protected by the patent...exists or is in the process of being established" in the United States. 19 U.S.C. § 1337(a)(2) (2008). Under Commission precedent, the domestic industry requirement of Section 337 consists of an "economic prong" and a "technical prong." *Certain Data Storage Systems and Components Thereof*, Inv. No. 337-TA-471, Initial Determination Granting EMC's Motion No. 471-8 Relating to the Domestic Industry Requirement's Economic Prong (unreviewed) at 3 (Public Version, October 25, 2002).

The "economic prong" of the domestic industry requirement is satisfied when it is determined that the economic activities set forth in subsections (A), (B), and/or (C) of subsection 337(a)(3) have taken place or are taking place. *Certain Variable Speed Wind Turbines and*

Components Thereof, Inv. No. 337-TA-376, USITC Pub. No. 3003, 1996 ITC LEXIS 556, Comm'n Op. at 21 (Nov. 1996). With respect to the "economic prong," 19 U.S.C. § 1337(a)(2) and (3) provide, in full:

> (2) Subparagraphs (B), (C), (D), and (E) of paragraph (1) apply only if an industry in the United States, relating to the articles protected by the patent, copyright, trademark, mask work, or design concerned, exists or is in the process of being established.
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> (3) For purposes of paragraph (2), an industry in the United States shall be considered to exist if there is in the United States, with respect to the articles protected by the patent, copyright, trademark, mask work, or design concerned-
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> (A) significant investment in plant and equipment;
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> (B) significant employment of labor or capital; or
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> (C) substantial investment in its exploitation, including engineering, research and development, or licensing.

Given that these criteria are listed in the disjunctive, satisfaction of any one of them will be sufficient to meet the domestic industry requirement. *Certain Integrated Circuit Chipsets and Products Containing Same*, Inv. No. 337-TA-428, Order No 10, Initial Determination (Unreviewed) (May 4, 2000), citing *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, Commission Op. at 15, USITC Pub. 3003 (Nov. 1996).

To meet the technical prong, the complainant must establish that it practices at least one claim of the asserted patent. *Certain Point of Sale Terminals and Components Thereof*, Inv. No. 337-TA-524, Order No. 40 (April 11, 2005). "The test for satisfying the 'technical prong' of the industry requirement is essentially same as that for infringement, i.e., a comparison of domestic products to the asserted claims." *Alloc v. Int'l Trade Comm'n*, 342 F.3d 1361, 1375 (Fed. Cir. 2003). The technical prong of the domestic industry can be satisfied either literally or under the doctrine of equivalents. *Certain Excimer Laser Systems for Vision Correction Surgery and*

Components Thereof and Methods for Performing Such Surgery, Inv. No. 337-TA-419, Order No. 43 (July 30, 1999).

A complainant who seeks to satisfy the domestic industry requirement by its investments in patent licensing must first establish that its asserted investment activities satisfy three requirements of section 337(a)(3)(C): that there is a nexus between relied upon investment activities and the asserted patents, that the investment relates to licensing, and that the investment occurred in the United States. *Certain Multimedia Display and Navigation Devices and Systems, Components Thereof, and Products Containing Same*, Inv. No. 337-TA-694, Commission. Op. at 7-8 (August 8, 2011) ("*Navigation Devices*"). Section 337(a)(3)(C) then requires the complainant to show that the qualifying investments are substantial. *Id.* at 8. Thus, where a complainant is relying on licensing activities, the domestic industry determination does not require a separate technical prong analysis and the complainant need not show that it or one of its licensees practices the patents-in-suit. *See Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing Same*, Inv. No. 337-TA-605, Initial Determination at 112 (February 9, 2009) (unreviewed in relevant part).

B. Analysis

Freescale's Position: Freescale contends that it satisfies the domestic industry requirement based on its domestic licensing activities related to the '455 patent.

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Freescale claims that it has had great success in licensing its patent portfolio. {

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Freescale asserts that the Commission has already found a domestic industry for the '455 patent based on Freescale's licensing activities. Freescale notes that the Commission declined to review Chief Judge Luckern's determination that Freescale made a substantial investment in licensing with respect to the '455 patent. (Citing CX-2C; CX-3.) Freescale argues that the evidence supports a finding that there is a strong nexus between Freescale's licensing activities

and the '455 patent, Freescale's domestic activities relate to the licensing of the '455 patent, Freescale's activities have a nexus to the United States, and Freescale's licensing investments are substantial.

Respondents' Position: Respondents contend that Freescale failed to prove that it meets the domestic industry requirement based on its licensing activities.

Respondents argue that Freescale failed to offer any evidence on any of the five factors relating to the nexus between the claimed investment and the '455 patent that were specifically called out in Order No. 19. Respondents claim that Freescale instead offered a witness statement that simply re-packaged the prior deficient information it submitted with its summary determination motion.

According to Respondents, the following alleged facts demonstrate that Freescale failed to satisfy the domestic industry requirement:

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Respondents argue that the evidence shows that Freescale does not license its patents for "industry-creating" or "production-driven" reasons, but to extract royalties for its "revenue-driven" licensing model. (Citing JX-16C at 77:11-18; JX-21C at 17:24-18:10.) Respondents argue that the Commission has articulated that this is not the type of activity that Congress intended to protect through Section 337.

Staff's Position: Staff contends that Freescale failed to prove that it meets the domestic industry requirement based on its licensing activities.

Staff notes that Order No. 19 raised questions relating to the domestic industry analysis that were not answered in Freescale's motion for summary determination. Staff argues that the evidence offered by Freescale fails to answer the questions raised by Order No. 19.

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Discussion and Conclusions: Based on the evidence in the record, I find that Freescale has not demonstrated that it satisfies the domestic industry requirement for the '455 patent based on its licensing activities.

Freescale seeks a finding that it has satisfied the domestic industry requirement under 19 U.S.C. § 1337(a)(3)(C) based on its licensing activities. This raises an issue that the Commission recently addressed – how to analyze licensing investments related to a patent portfolio when the asserted patent is only a subset of that portfolio.

In *Certain Multimedia Display & Navigation Devices & Systems, Components Thereof, & Products Containing Same*, Inv. No. 337-TA-694, Comm'n Op. (Aug. 8, 2011) ("*Navigation Devices*"), the Commission stated that a complainant seeking to rely on licensing activities must satisfy three requirements: (1) the investment must be "an investment in the exploitation of the asserted patent;" (2) the investment must relate to licensing; and (3) the investment "must be domestic, *i.e.*, it must occur in the United States." *Id.* at 7-8. The Commission stated that "[o]nly after determining the extent to which the complainant's investments fall within these statutory parameters can we evaluate whether complainant's qualifying investments are 'substantial,' as required by the statute." *Id.* at 8. I will address each of these three factors, and then address whether or not Freescale's investments are "substantial" pursuant to the statute.

Nexus to the '455 Patent

In *Navigation Devices*, the Commission explained that because the complainant's "activities are associated both with the asserted patents and unasserted patents, a key issue presented is the strength of the nexus between the activities and the asserted patents." *Navigation Devices* at 8. When the asserted patent is part of a patent portfolio, and the licensing activities relate to the portfolio as a whole, the Commission requires that the facts be examined

to determine the strength of the nexus between the asserted patent and the licensing activities. *Id.* at 8-9.

The Commission provided a non-exhaustive list of factors to consider, such as (1) whether the licensee's efforts relate to "an article protected by" the asserted patent under Section 337 (a)(2)-(3); (2) the number of patents in the portfolio; (3) the relative value contributed by the asserted patent to the portfolio; (3) the prominence of the asserted patent in licensing discussions, negotiations, and any resulting licensing agreement; and (4) the scope of technology covered by the portfolio compared to the scope of the asserted patent. *Id.* at 9-10. The Commission explained that the asserted patent may be shown to be particularly important or valuable within the portfolio where there is evidence that: (1) it was discussed during licensing negotiations; (2) it has been successfully litigated before by the complainant; (3) it is related to a technology industry standard; (4) it is a base patent or pioneering patent; (5) it is infringed or practiced in the United States; or (6) the market recognizes the patent's value in some other way. *Id.* at 10-11.

I find that there is a nexus between Freescale's licensing activities and the '455 patent.

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} Freescale's Law Director of Intellectual Property Licensing, Mr. Lee Chastain, understands a "patent family" to consist of "a group of related patents, typically an originally filed in other countries...and also continuations, divisionals, re-examinations." (JX-16C at 22:18-24.) Mr.

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} Freescale enters into licenses with semiconductor manufacturers, electronic devices manufacturers, and, in limited situations, foundry companies. (*Id.* at Q. 32-36.) {

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I find that the relative value of the '455 patent to Freescale's patent portfolio can be seen in the emphasis placed on the '455 patent during licensing negotiations. {

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During negotiations, Freescale offered the potential licensee a presentation that outlines representative claims of the '455 patent, and an explanation of why Freescale believed that those claims read on the licensees' products. (*See, e.g.,* CX-36C, CX-43C.) {

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Freescale argues that the nexus is shown by Freescale's success in litigating the '455 patent. (CIB at 77-78.) I do not concur with Freescale that there is evidence that the '455 patent has been successfully litigated. {

} I find that the fact that Freescale's litigation with Panasonic resulted in a favorable settlement does not demonstrate that the '455 patent "has been successfully litigated before by" Freescale as the Commission envisioned in *Navigation Devices*. There is no evidence to support a finding of why the parties settled, and Panasonic's decision to settle and take a license may have related to business reasons beyond the alleged strength of the '455 patent.

Freescale also cites to the 709 Investigation, claiming that had Chief Judge Luckern found the Zoran documents he reviewed to be authentic and reliable, he would have found the accused products to infringe the '455 patent. (CIB at 78.) I find that this assertion is irrelevant, because Chief Judge Luckern's ultimate conclusion in the 709 Investigation was a finding of no violation of Section 337 based on Freescale's failure to prove infringement. (CX-65.) This finding was upheld by the Commission. Therefore, the 709 Investigation cannot be considered a successful litigation pursuant to *Navigation Devices*.

{

} I find that Freescale's evidence on this issue is insufficient. Freescale cites to its Complaints in this investigation and the 709 Investigation, where it alleged that the '455 patent related to the DDR2 standard. Freescale cites to claim charts that it prepared for licensing negotiations that compared the '455 patent to data sheets for the DDR2 memory standard. Neither of these constitute sufficient evidence to demonstrate that

the '455 patent is related to the DDR2 memory standard. {

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Freescale argues that the nexus is shown by the fact that the '455 patent is infringed and practiced in the United States. As discussed in Section VI *supra*, Freescale has demonstrated that the Accused Zoran Resistor Termination Products infringe claims 9 and 10 of the '455 patent. This evidence supports a finding of nexus according to *Navigation Devices*.

Freescale argues that the nexus is shown by the fact that Freescale's licensing efforts relate to articles protected by the '455 patent. As support for this, Freescale points to the fact that many companies that have licensed the '455 patent manufacture products. Freescale also points to the fact that in the licensing negotiations, Freescale identified representative products of the licensees that allegedly infringed the '455 patent. (*See, e.g.*, CX-46C.)

I find that the fact that Freescale asserted the '455 patent against certain products found in the United States, and that companies took a license to the '455 patent, does not demonstrate that Freescale's licensing efforts relate to articles protected by the '455 patent. There has been no evidence offered that any of the licensees' products actually practice the '455 patent. Freescale's bare-bones license presentations containing infringement allegations are insufficient to prove this point. (*Id.*)

Based on the foregoing, I find that there is a nexus between Freescale's licensing activities and the '455 patent. Respondents and Staff note that there are multiple factors identified by the Commission that are not proven by Freescale. While this is correct, I find that this does not preclude a finding of nexus. The factors identified by the Commission are merely guidelines for determining nexus, and there is no requirement that a certain number of them must

be met before a finding of nexus can be made. *Navigation Devices*, at 8-12. I find that the evidence addressed *supra* is sufficient to demonstrate nexus, regardless of the fact that Freescale has not proven each and every factor articulated by the Commission in *Navigation Devices*.

Relation of Freescale's Activities to Licensing

The Commission has explained that "section 337(a)(3)(C) also requires [a] complainant's activities to relate to licensing." *Navigation Devices*, at 14. The Commission noted that "[s]ome activities are *solely* related to licensing while others can serve multiple purposes." *Id.* (emphasis in original).

It cannot be disputed that Freescale's activities relate to licensing. {

} These employees were and are in charge of administration and oversight of the patent portfolio, monitoring the marketplace for potential infringers, conducting technical analyses of potentially infringing products, conducting licensing negotiations, drafting license agreements, and providing legal and accounting/finance support. (*Id.* at Q. 13.) Freescale incurred costs related to the salary of these employees and non-salary costs related to licensing. (*Id.* at Q. 17-28.) {

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} I find that Respondents' argument goes to whether or not Freescale's investment in licensing is substantial, an issue addressed *infra*. Respondents do not dispute that Freescale conducts

domestic activities related to licensing, and I find that Freescale has satisfied this nexus requirement.

Investment Occurring in the United States

The Commission has explained that "[t]he most obvious requirement of section 337(a)(3) is that the investment occur in the United States." *Navigation Devices*, at 14. In addressing the issue in the context of licensing, the Commission stated:

> ***When a complainant's licensing activity is performed and directed within the United States, this weighs in favor of a strong nexus between the activities and the United States.*** The Commission's analysis is a fact-focused and case-specific inquiry that takes into account the extent to which the complainant conducts its licensing operations in the United States, including the employment of U.S. personnel and utilization of U.S. resources in its licensing activities.

Id. at 14-15 (emphasis added).

I find that Freescale's licensing activities include investment occurring in the United States. Freescale's licensing activities are directed from its headquarters in Austin, Texas. (CX-402C at Q. 12.) Freescale's employees that work on licensing issues are employed within the United States. (*Id.* at Q. 13.) Freescale incurs costs in the United States related to the employees' salaries and other non-salary costs. (*Id.* at Q. 22, 26-28.)

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} This issue will be addressed more fully in the substantiality analysis *infra*. Still, I find that this fact does not preclude the conclusion that Freescale's licensing activities include investments occurring in the United

States. There is no requirement that all of Freescale's activities occur in United States. The fact that Freescale runs its licensing operation in the United States, employs individuals in the United States who work on the licensing operation, and incurs costs related to the licensing operation in the United States is sufficient to find investment occurring in the United States.

Whether or Not the Investment is Substantial

In order to prove the existence of a domestic industry based on licensing activities, a complainant must demonstrate a "substantial investment" related to those activities. 19 U.S.C. § 1337(a)(3)(C). In addressing the substantiality requirement in the situation where the asserted patent is part of a larger patent portfolio, the Commission has explained:

> In performing our analysis, we adopt a flexible approach whereby a complainant whose showing on one or more of the three section 337(a)(3)(C) requirements is relatively weak may nevertheless establish that its investment is "substantial" by demonstrating that its activities and/or expenses are of a large magnitude. The Commission has indicated that whether an investment is substantial may depend on the industry and the size of the complainant. The type of efforts that are considered a "substantial investment" under section 337(a)(3)(C) will vary depending on the nature of the industry and the resources of the complainant.
>
> Other factors that might be relevant in determining whether a complainant's investment is substantial are (1) the existence of other types of "exploitation" of the asserted patent such as research, development, or engineering, (2) the existence of license-related ancillary activities such as ensuring compliance with license agreements and providing training or technical support to its licensees, (3) whether complainant's licensing activities are continuing, and (4) whether complainant's licensing activities are those that are referenced favorably in the legislative history of section 337(a)(3)(C). The complainant's return on its licensing investment (or lack thereof) may also be circumstantial evidence of the complainant's investment.

Navigation Devices, at 15-16 (citations omitted).

Freescale relies on the investments it makes in salary for U.S. employees involved in licensing efforts. {

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} Freescale asserts that all of these expenditures should be counted in the domestic industry analysis.

Respondents and Staff argue that not all of the salary costs should count towards the domestic industry analysis. They claim that Freescale has not attempted to exclude the portions of the salaries properly apportioned to litigation and other non-licensing activities.

In listing the salaries to be included in the domestic industry calculation, Freescale included the employees' full salaries. (JX-16C at 125:1-6.) {

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I concur with Respondents and Staff that it is improper to include the employees' full salaries in the calculation when Freescale admits that not every employee identified by Mr. Chastain spends all of his/her time working on licensing issues. The only relevant concern is the extent of Freescale's investment relating to licensing, and those portions of salary paid to employees to perform tasks unrelated to licensing shall not be included in the analysis. This is akin to the understanding for the economic prong under subsections (A) and (B) that the only relevant investment is the one related to the alleged domestic industry product(s), as opposed to a

complainant's products as a whole. *See Certain Printing & Imaging Devices & Components Thereof*, Inv. No. 337-TA-690, Order No. 24 (Apr. 21, 2010) (instructing the parties that "domestic industry allegations must be specifically tied to the product(s) asserted to practice the patents, rather than generally referencing the investments related to all" products); *Certain Digital Televisions & Certain Products Containing Same & Methods of Using Same*, Inv. No. 337-TA-617, Order No. 54 (July 1, 2008) (finding that "the lack of information concerning the allocation of expenditures and activities prevents the granting of summary determination.") Freescale's failure to provide its investments in salary tied only to the licensing activities of its employees precludes me from determining whether or not Freescale's actual investment in employee salary related to licensing is in fact "substantial" pursuant to Section 337.[13]

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} I find that this testimony is insufficient to establish "substantial investment" for at least three reasons.

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} Therefore, knowing the extent to which each listed individual works on licensing matters is important, as not every salary in the list is equal. Finally, the fact that an employee is a member of the Intellectual Property Licensing Group does not ensure that he spends 100% of

[13] By contrast, I found that the complainant in another investigation proved the domestic industry requirement through its licensing activities when the asserted patents were part of a larger patent portfolio. *Certain Liquid Crystal Display Devices, Including Monitors, Televisions, & Modules, & Components Thereof*, Inv. Nos. 337-TA-749, 337-TA-741, Initial Determination (Jan. 12, 2012). There, the complainant offered testimony regarding the percentage of time that the relevant employees devoted to the complainant's licensing efforts. *Id.* at 426-428.

his time on licensing matters. {

} Therefore, Mr. Chastain's testimony does not cure the lack of detail provided by Freescale.[14]

Freescale also relies on non-payroll investments. {

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[14] In addition to citing to Question 19 of CX-402C, Freescale cites to various portions of Mr. Chastain's deposition testimony. (CRB at 47.) None of these citations to the deposition testimony provide any support for the allegation that the employees of the Intellectual Property Group spend 100% of their time working on licensing matters.

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The parties dispute whether or not the costs related to the reverse engineering work performed outside of the U.S. can be counted for purposes of the domestic industry analysis. I find that Freescale's expenditures on reverse engineering work done outside of the U.S. cannot count towards domestic industry. Work done outside of the U.S., even if it is for the benefit of a company headquartered in Texas, does not qualify as a domestic investment.

Freescale claims that "even if some reverse engineering work is performed outside the U.S., that work is performed under contracts entered into in the U.S., and the resulting reports are used by Freescale employees for licensing operations." (CRB at 48.) Accepting Freescale's argument would allow all international expenditures to be counted if they were financed by or for the benefit of a U.S. entity. For example, all manufacturing costs for a factory outside of the U.S. would count towards the domestic industry analysis if the factory was paid by a U.S. entity and produced goods for the benefit of a U.S. entity. I find that such a result would not be consistent with Section 337.

Because Freescale failed to provide any evidence regarding which reverse engineering costs relate to U.S. activities versus foreign activities, those costs shall not be included in the domestic industry calculation. Turning to the chart of Freescale's non-payroll costs, {

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Based upon the foregoing, I find that the "Ext Services" and "Depreciation" rows in the chart shall not be counted towards Freescale's non-payroll domestic industry expenditures.

{

} Freescale is a large corporation with over $4 billion in "net sales" at a cost of approximately $2.7 billion in 2010, and the semiconductor industry was a $212.77 billion industry in 2010. (RX-156 at 5, 35.) {

} The Commission has determined that "whether an investment is substantial may depend on the industry and the size of the complainant." *Navigation Devices*, at 15. I find that the investments demonstrated in this case, on their own, are not substantial. (*Id.*)

Next, I turn to the other factors that the Commission stated "might be relevant in determining whether a complainant's investment is substantial." *Navigation Devices*, at 16. These consist of: (1) the existence of other types of "exploitation" of the asserted patent such as research, development, or engineering; (2) the existence of license-related activities such as ensuring compliance with license agreements or providing training and technical support; (3) whether the licensing activities are continuing; and (4) whether the licensing activities are those that are referenced favorably in the legislative history of Section 337. *Id.*

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Freescale's licensing efforts are continuing. (*See generally* CX-402C.) Respondents do not dispute this point. (ZIB at 55.)

Regarding the fourth factor identified by the Commission, Freescale admits that its goal in licensing its patent portfolio is to generate revenue from its intellectual property. (JX-21C at 17:24-18:10.) Freescale's business model involves examining existing products for possible infringement, and then approaching alleged infringers to negotiate a license. (*See* CX-402C at Q. 26-27, 57-60.) Freescale's activities therefore "reflect a revenue-driven licensing model targeting existing production rather than the industry-creating, production-driven licensing activity that Congress meant to encourage." *Navigation Devices*, at 25.

The only factor of the four identified by the Commission that favors Freescale is the fact that Freescale's licensing efforts are continuing. I find that this alone is not enough to support a finding that the investment described *supra* is "substantial" within the meaning of Section 337. Based on the foregoing, I find that Freescale has not met its burden to demonstrate that it has made a "substantial investment" in licensing as required by 19 U.S.C. § 1337(a)(3)(C). Therefore, I find that Freescale failed to satisfy the domestic industry requirement.

VIII. REMEDY & BONDING

A. Limited Exclusion Order

Freescale's Position: Freescale contends that it is entitled to a limited exclusion order directed at the products of the Respondents found to have infringed one or more claims of the '455 patent.

Respondents' Position: Respondents contend that Freescale is not entitled to any exclusion order. If the Commission issues an exclusion order, Respondents claim that it should be a limited exclusion order, and not a general exclusion order. Respondents assert that any limited exclusion order should not include any Funai television, should include a certification provision, and should include an exception to allow for service and repair of any product sold before the date of issuance of the exclusion order.

Staff's Position: Staff contends that if a violation is found, a limited exclusion order should issue baring importation and sale of all infringing integrated circuits or chip sets manufactured by or on behalf of Respondents that are imported by, for, or on behalf of Respondents. Staff agrees that any limited exclusion order should include the three conditions raised by Respondents.

Discussion and Conclusions: I have found that, in this case, there is no violation of Section 337. Should the Commission find a violation of Section 337, however, I recommend that the Commission issue a limited exclusion order that applies to the Respondents found to infringe the '455 patent as well as all of their affiliated companies, parents, subsidiaries, or other related business entities, or their successors or assigns, and covers the certain integrated circuits, chipsets, and products containing same including televisions found to infringe the asserted patents.

I recommend that any limited exclusion order include a certification provision. Freescale does not oppose this request. The Commission has explained that "[c]ertification provisions are generally included in exclusion orders where Customs is unable to easily determine by inspection whether an imported product violates a particular exclusion order." *Certain Semiconductor Chips With Minimized Chip Package Size & Products Containing Same*, Inv. No. 337-TA-605, Commission Opinion (July 29, 2009) (including a certification provision in an exclusion order because of the difficulty of determining whether imported products contain the infringing chipsets); *see also Certain Ground Fault Circuit Interrupters & Products Containing Same*, Inv. No. 337-TA-615, Commission Opinion (Mar. 26, 2009) (noting that a certification provision "gives U.S. Customs & Border Protection the authority to accept a certification from the parties that goods being imported are not covered by the exclusion order.") Here, because Customs would not be able to easily determine by inspection whether or not an imported product violates the exclusion order, I find that a certification provision is appropriate.

I recommend that any exclusion order include an exception to allow importation of service and replacement parts purchased prior to the issuance of the exclusion order. Freescale does not oppose this request. The Commission has found in the past that the public interest weighs in favor of such an exception. *Certain Liquid Crystal Display Devices & Products Containing the Same*, Inv. No. 337-TA-631, Comm'n Op. at 27 (July 14, 2009.)

I recommend that any limited exclusion order take into consideration Funai, as Funai was terminated from this investigation via a consent order. The consent order issued by the Commission allows Funai to import, sell for importation, or sell in the U.S. after importation products alleged to infringe claims 9 and 10 of the '455 patent until May 1, 2013. Any limited exclusion order should not contradict this consent order that is already in place.

B. Cease & Desist Order

Freescale's Position: Freescale contends that a cease and desist order directed to Zoran is appropriate because Zoran maintains a commercially significant inventory of accused products within the United States. Freescale states that Zoran has at least { } total units stored in a warehouse in Sunnyvale, California. (Citing CX-274C at ¶¶ 10-12; CX-91C; CX-306C; CX-310C.) Freescale does not request a cease and desist order with respect to MediaTek.

Zoran's Position: Zoran contends that Freescale failed to show the requisite conditions for a cease and desist order. Zoran asserts that the { } units that Zoran holds in California do not amount to a commercially significant inventory. (Citing CX-274C at ¶¶ 10-12.)

Staff's Position: Staff contends that Freescale has failed to demonstrate that it is entitled to a cease and desist order directed to Zoran. Staff asserts that Zoran's inventory of { } products does not amount to a commercially significant inventory.

Discussion and Conclusions: I have found that, in this case, there is no violation of Section 337. Should the Commission find a violation of Section 337, however, I do not recommend the entry of a cease and desist order against Zoran.

Section 337 provides that the Commission may issue a cease and desist order as a remedy for violation of Section 337. *See* 19 U.S.C. § 1337(f)(1). The Commission generally issues a cease and desist order directed to a domestic respondent when there is a "commercially significant" amount of infringing, imported product in the United States that could be sold so as to undercut the remedy provided by an exclusion order. *See Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, USITC Pub. 2391, Comm'n Op. on Remedy, the Public Interest and Bonding at 37-42 (June 1991); *Certain Condensers, Parts Thereof and Products Containing Same, Including Air Conditioners for Automobiles*, Inv. No. 337-TA-334, Comm'n

Op. at 26-28 (Aug. 27, 1997). The complainant bears the burden of proving that a respondent has a commercially significant inventory in the United States. *Certain Integrated Repeaters, Switches, Transceivers & Products Containing Same*, Inv. No. 337-TA-435, Comm'n Op., 2002 WL 31359028 (Aug. 16, 2002).

The parties stipulated that at least { } total units of the Accused Zoran Products have been stored in a warehouse in California since October 1, 2010. (CX-274C at ¶ 12.) The parties' stipulation defines "Accused Zoran Products" to include products that I have deemed are precluded from this investigation. (*Compare* CX-274C at ¶2 *with* Section V, *supra*.) Therefore, it is unknown how many non-precluded products are currently held by Zoran in the United States.

Even if Zoran currently holds { } non-precluded products in the U.S., I do not find that an inventory of { } Zoran chips, on its face, constitutes a commercially significant inventory. Freescale offers no argument or explanation regarding why the inventory of { } products constitutes a commercially significant inventory. (CIB at 99.) Therefore, I find that Freescale failed to meet its burden on this issue. I decline to recommend entry of a cease and desist order against Zoran.

C. Bonding

Freescale's Position: Freescale contends that a bond of 100% of the entered value for any importation of infringing products should be imposed in this case.

Freescale contends that the number of products is significant and not amenable to an easy price comparison because Respondents import and/or sell dozens of different models and set a wide range of prices for the exact same product depending on various factors. (Citing CX-274C.) Freescale asserts that a 100% bond is necessary to protect Freescale's licensing industry

from harm. Freescale claims that if Respondents are allowed to continue importing during the Presidential review period without a bond, Freescale's licensing efforts will be adversely affected because products adjudged to infringe for which no royalty is being paid will be flooding into the market.

Respondents' Position: Respondents contend that Freescale failed to establish the need for a bond.

Respondents assert that Freescale did not demonstrate that any bond is necessary to protect it from injury. Respondents state that Freescale offered no evidence demonstrating that Respondents enjoy any competitive advantage that, in the absence of a bond, will result in injury to Freescale. Respondents state that Freescale did not carry its burden of presenting evidence to support any bond amount.

Staff's Position: Staff contends that Freescale failed to establish the need for a bond. Staff states that Freescale failed to submit evidence needed to calculate a bond based on a reasonable royalty rate. Therefore, Staff believes that no bond should be set during the Presidential review period.

Discussion and Conclusions: I have found that, in this case, there is no violation of Section 337. Should the Commission find a violation of Section 337, however, I recommend that no bond be required.

The administrative law judge and the Commission must determine the amount of bond to be required of a respondent, pursuant to section 337(j)(3), during the 60-day Presidential review period following the issuance of permanent relief, in the event that the Commission determines to order a remedy. The purpose of the bond is to protect the complainant from any injury. 19 CFR §§ 210.42(a)(1)(ii), 210.50(a)(3). The complainant has the burden of supporting any

bond amount it proposes. *Certain Rubber Antidegradants, Components Thereof, and Products Containing Same*, Inv. No. 337-TA-533, Comm'n Op., 2006 ITC LEXIS 591 (Jul. 21, 2006).

When reliable price information is available, the Commission has often set the bond by eliminating the differential between the domestic product and the imported, infringing product. *See Certain Microsphere Adhesives, Processes for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes*, Inv. No. 337-TA-366, Comm'n Op. a 24 (1995). In other cases, the Commission has turned to alternative approaches, especially when the level of a reasonable royalty rate could be ascertained. *See, e.g., Certain Integrated Circuit Telecommunication Chips and Products Containing Same, Including Dialing Apparatus*, Inv. No. 337-TA-337, Comm'n Op. at 41 (1995).

The Commission has set a bond of 100% when the evidence supported a finding that it would be difficult or impossible to calculate a bond based on price differentials. *Certain Variable Speed Wind Turbines and Components Thereof*, Inv. No. 337-TA-376, Comm'n Op., 1996 WL 1056209 (Sept. 23, 1996) (finding that a bond of 100% was appropriate "because of the difficulty in quantifying the cost advantages of respondents' imported Enercon E-40 wind turbines and because of price fluctuations due to exchange rates and market conditions."); *Certain Systems For Detecting and Removing Viruses or Worms, Components Thereof, and Products Containing Same*, Inv. No. 337-TA-510, Comm'n Op., 2007 WL 4473083 (Aug. 2007) (imposing a bond of 100% based on a finding that the parties had numerous models and products lines, and that a price comparison would be difficult because respondent's products were a combination of hardware and software while the complainant's products were software only); *Certain Flash Memory Circuits and Products Containing Same*, Inv. No. 337-TA-382, USITC Pub. No. 3046, Comm'n Op. at 26-27 (July 1997) (a 100% bond imposed when price

comparison was not practical because the parties sold products at different levels of commerce, and the proposed royalty rate appeared to be *de minimis* and without adequate support in the record).

I find that Freescale has failed to establish that a bond is appropriate. "The purpose of a bond during the Presidential review period is to offset any competitive advantage resulting from the alleged unfair acts enjoyed by persons benefitting from the importation of the articles in question." *Certain Silica-Coated Lead Chromate Pigments*, Inv. No. 337-TA-120, Views of the Comm'n (Apr. 21, 1983). Freescale focuses on licensing the '455 patent, and it does not claim to manufacture, market, or sell any products that practice the '455 patent. (JX-21C at 17:24-18:10; JX-16C at 204:6-20, 205:8-10, 205:25-206:5, 206:18-20.) Freescale argues that allowing Respondents to import products during the Presidential review period without a bond will harm Freescale's licensing business, but Freescale offers no evidence to support this claim. (CIB at 100.) "Attorneys' argument is no substitute for evidence." *Johnston v. IVAC Corp.*, 885 F.2d 1574, 1581 (Fed. Cir. 1989). Therefore, I find that Freescale failed to meet its burden to demonstrate that a bond is necessary should the Commission find a violation of Section 337.

IX. MATTERS NOT DISCUSSED

This Initial Determination's failure to discuss any matter raised by the parties, or any portion of the record, does not indicate that it has not been considered. Rather, any such matter(s) or portion(s) of the record has/have been determined to be irrelevant, immaterial or meritless. Arguments made on brief which were otherwise unsupported by record evidence or legal precedent have been accorded no weight.

X. CONCLUSIONS OF LAW

1. The Commission has subject matter jurisdiction, *in rem* jurisdiction, and *in personam*

jurisdiction.

2. There has been an importation into the United States, sale for importation, or sale within the United States after importation of the accused integrated circuits, chipsets, and products containing same including televisions, which are the subject of the alleged unfair trade allegations.

3. An industry does not exist in the United States that exploits U.S. Pat. No. 5,467,455, as required by 19 U.S.C. § 1337(a)(2).

4. Claims 9 and 10 of U.S. Pat. No. 5,467,455 are not invalid pursuant to 35 U.S.C. § 102.

5. Claims 9 and 10 of U.S. Pat. No. 5,467,455 are invalid pursuant to 35 U.S.C. § 103.

6. The accused MediaTek products do not infringe claims 9 and 10 of U.S. Pat. No. 5,467,455.

7. Pursuant to the doctrine of issue preclusion, Freescale is precluded from asserting that the following Zoran products infringe claims 9 and 10 of U.S. Pat. No. 5,467,455: ZR39770BGCF; ZR39772HGCF-B; ZR39775HGCF-B; ZR39775HGCF-TC; ZR39775HGCF-TC-LP; ZR39785HGCF-B; ZR39787HGCF; and ZR39787HGCF-LP.

8. The ZR39760HGCF-A1, ZR39775HGCF-BD, ZR39780HGCF, ZR39785HGCF-BD, and ZR39788HGCG Zoran products infringe claims 9 and 10 of U.S. Pat. No. 5,467,455.

9. There is no violation of 19 U.S.C. § 1337(a)(1) with respect to U.S. Pat. No. 5,467,455.

XI. ORDER

Based on the foregoing, and the record as a whole, it is my Final Initial Determination that there is no violation of 19 U.S.C. § 1337(a)(1) in the importation into the United States, sale

for importation, and the sale within the United States after importation of certain integrated circuits, chipsets, and products containing same including televisions.

I hereby **CERTIFY** to the Commission my Final Initial and Recommended Determinations together with the record consisting of the exhibits admitted into evidence. The pleadings of the parties filed with the Secretary, and the transcript of the pre-hearing conference and the hearing, as well as other exhibits, are not certified, since they are already in the Commission's possession in accordance with Commission rules.

It is further **ORDERED** that:

In accordance with Commission Rule 210.39, all material heretofore marked *in camera* because of business, financial and marketing data found by the administrative law judge to be cognizable as confidential business information under Commission Rule 201.6(a), is to be given *in camera* treatment continuing after the date this investigation is terminated.

The initial determination portion of the Final Initial and Recommended Determination, issued pursuant to Commission Rule 210.42(a)(1)(i), shall become the determination of the Commission sixty (60) days after the service thereof, unless the Commission, within that period, shall have ordered its review of certain issues therein, or by order, has changed the effective date of the initial determination portion. If the Commission determines that there is a violation of 19 U.S.C. § 1337(a)(1), the recommended determination portion, issued pursuant to Commission Rule 210.42(a)(1)(ii), will be considered by the Commission in reaching a determination on remedy and bonding pursuant to Commission Rule 210.50(a).

On or before July 24, 2012, the parties shall submit to the Office of Administrative Law

Judges ***a joint statement*** regarding whether or not they seek to have any portion of this document deleted from the public version. The parties' submission shall be made by hard copy and must include a copy of this Initial Determination with red brackets indicating any portion asserted to contain confidential business information to be deleted from the public version. The parties' submission shall include an index identifying the pages of this document where proposed redactions are located. The parties' submission concerning the public version of this document need not be filed with the Commission Secretary.

SO ORDERED.

Issued: 7/12/2012
DATE

Robert K. Rogers, Jr.
Administrative Law Judge

CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS

Inv. No. 337-TA-786

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **INITIAL DETERMINATION** was served upon **Juan S. Cockburn, Esq.,** Commission Investigative Attorney, via hand, and the following parties via first class mail delivery on

AUG 20 2012

Lisa R. Barton, Acting Secretary
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CERTAIN INTEGRATED CIRCUITS, CHIPSETS, AND PRODUCTS CONTAINING SAME INCLUDING TELEVISIONS

Inv. No. 337-TA-786

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