Dense Coding Demonstration and Microfabricated Ion Traps

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NIST National Institute of Standards and Technology

ARDA Advanced Research and Development Activity

National Security Agency

Quantum dense coding:

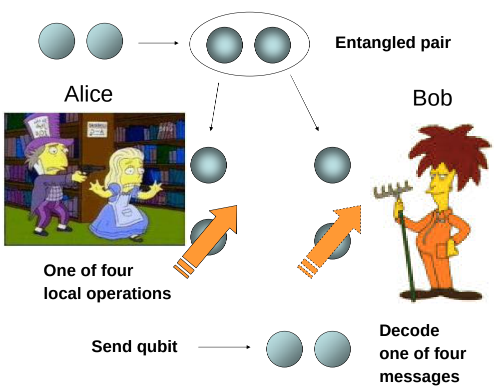
the communication of two bits of classical information through transmission of one quantum bit

(T. Schaetz, et al.)

Theoretically proposed
by Bennett and Wiesner (PRL **69** 2881 (1992))

Experimentally realized for photon 'trits'
by Mattle, Weinfurter, Kwiat, and Zeilinger (PRL **76** 4656 (1996))
- **Only two Bell states identifiable, other two indistinguishable (one trit, not two bits)**
- **Nondeterministic (30 photons pairs per trit)**

Scheme



Protocol

- **Produce entangled pair**
  - $\pi/2$-pulse and phase gate on two ions
- **Alice Rotates her qubit**
  - σ_X, σ_Y, σ_Z, or I (identity) on 1st ion, no operation on 2nd ion
- **Bob performs Bell state measurement**
  - Phase gate and $\pi/2$-pulse on both ions
- **Qubit detection**
  - Separate ions and read out ions' states individually

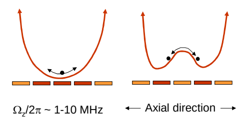
Experimental Results

	I	σ_X	σ_Y	σ_Z
↓↓	**0.84**	0.07	0.06	0.03
↑↓	0.02	0.03	0.08	**0.87**
↓↑	0.07	0.01	**0.84**	0.08
↑↑	0.08	**0.84**	0.04	0.04

Average fidelity: 85%

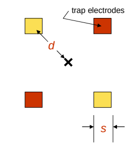
Why scale down?

- **Speed**: quantum logic gate speed prop. to motional frequency
- **Control**: for separation, smaller electrodes closer to ions



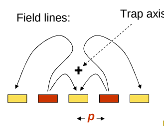
How small (or big)?

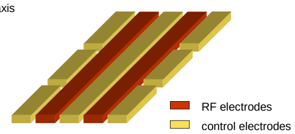
- Physical limitations
  - Laser beam waist size (~25 μm)
  - Heating
    - Fluctuating patch potentials (~ d^{-4})
    - Johnson noise (~ d^{-2} -- d^{-3})
- Fabrication size limitations
  - Precise control of dims. in 2D
    - Photolithography (~1 μm < s < ~ 1 cm)
  - Third dim. (s < ~ 3 μm, s > 0.3 mm), s ~ 10's μm: not easy

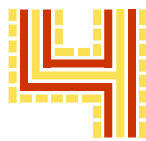


Planar surface trap geometry

(J. Chiaverini)

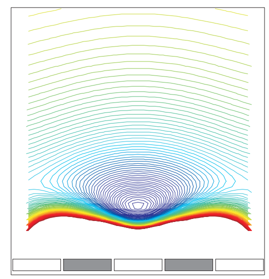






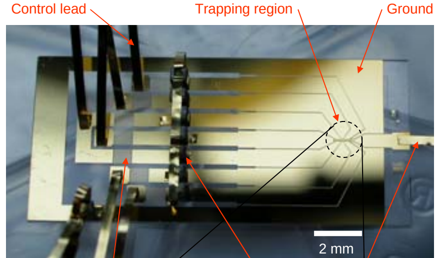
Elbows and tee-junctions possible

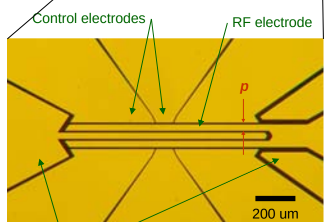
Pseudopotential contours of 5-wire geometry (RF potential between gray and white electrodes) plus axial potential



- Target parameters
  - RF amplitude V_0=100-200 V
  - RF drive frequency $\Omega/2\pi$ = 90 MHz
  - Electrode width w=40 μm
  - Trap axis above surface d=50-60 μm
  - Rad. secular frequency $\omega_r/2\pi$=15 MHz ($^9Be^+$)
  - Trap depth E_t=10^4 K

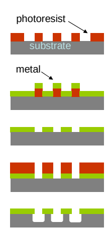
Micrographs of planar trap chip (gold on fused silica)





Fabrication

Liftoff with substrate etch



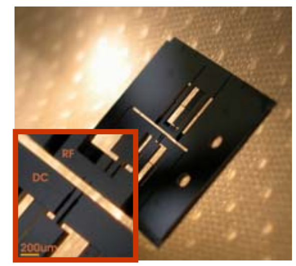
1. Coat substrate and define wire pattern in resist
2. Deposit metal
3. Remove resist
4. Coat and define trench pattern in resist
5. Etch trenches in substrate (RIE or HF) and remove resist

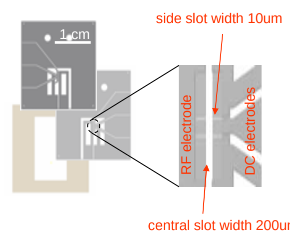
Parameter scaling

- Trap above surface: $d \sim p$
- Curvature at pseudopotential min.: $k \sim p^{-4}$
- Secular freq.: $\omega_r \sim p^{-2}$
- Trap depth: $E_t \sim p^{-2}$
- (RF potential, drive freq. kept constant)

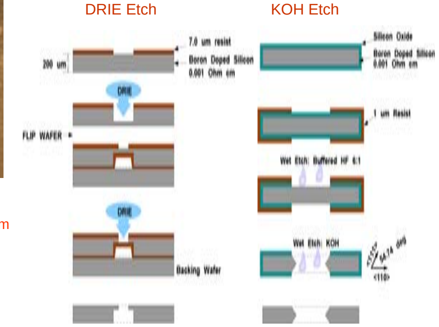
Silicon wafer trap, standard quadrupole geometry

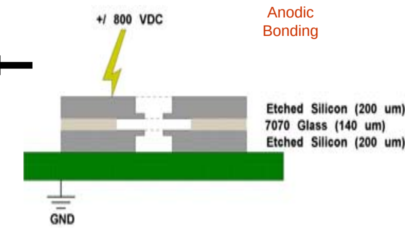
(J. Britton)



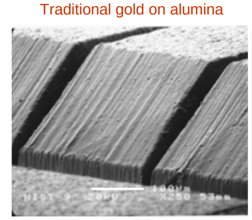


Fabrication

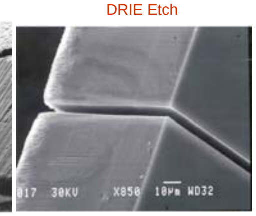




Traditional gold on alumina



DRIE Etch



KOH Etch