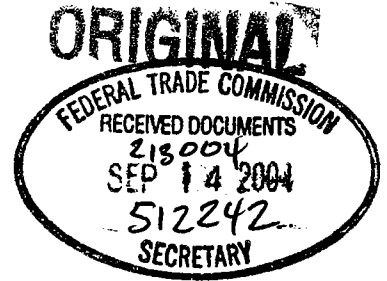


UNITED STATES OF AMERICA  
BEFORE FEDERAL TRADE COMMISSION



COMMISSIONERS: Deborah Platt Majoras, Chairman  
Orson Swindle  
Thomas B. Leary  
Pamela Jones Harbour  
Jon Leibowitz

In the Matter of

RAMBUS INCORPORATED,

a corporation.

Docket No. 9302

**PUBLIC**

**LIST OF EXHIBITS THAT MAY BE DISPLAYED OR OTHERWISE REFERRED TO  
DURING COMPLAINT COUNSEL'S TECHNOLOGY PRESENTATION**

Pursuant to the Commission's Order dated August 20, 2004, the following is the list of exhibits that Complaint Counsel expects to display or refer to during its technology presentation on September 21, 2004:

CX0234  
CX0371  
CX0424  
CX1309  
CX1454  
CX1460  
CX1543  
DX0001  
DX0013  
DX0049

DX0054  
DX0057  
DX0058  
DX0059  
DX0060  
DX0065  
DX0067  
DX0068  
DX0071  
DX0072  
DX0073  
DX0079  
DX0088  
DX0089  
DX0091  
DX0094  
DX0141  
DX0358  
DX0382  
JX0031  
JX0056

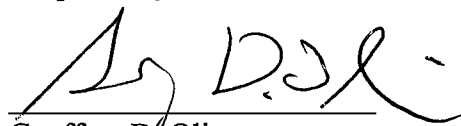
In addition, Complaint Counsel might refer to certain of the following exhibits,  
depending on the issues and questions that arise during the course of the proceeding.

CX0034  
CX0367  
CX0368  
CX1320  
CX3025 (in camera)  
DX0005  
DX0007  
DX0044  
DX0053  
DX0080  
DX0081  
DX0083  
DX0084  
DX0085  
DX0090  
DX0093

DX0100  
DX0105  
JX0010  
JX0028  
JX0029  
JX0031

Complaint Counsel has created two new demonstrative exhibits for use during technology day. Complaint Counsel has taken the multiple clock edges shown in DX0358 to create separate exhibits that identify and illustrate separately each of the clock edges. Complaint Counsel has also modified slightly images from CX0367, CX1543, DX0001, DX0065, DX0079, DX0088, DX0094, and selected pages of DX0382 in order to illustrate more clearly certain technological concepts. Certain pages of DX0382 and the clock slides derived from DX0358 have been modified to show movement. Copies of all such modified demonstrative exhibits, including those showing movement, are contained on the compact disk submitted with this filing.

Respectfully submitted,



Geoffrey D. Oliver  
Patrick J. Roach  
Robert P. Davis

Bureau of Competition  
Federal Trade Commission  
Washington, D.C. 20008  
(202) 326-2275  
Counsel for the Complaint

September 14, 2004

**CERTIFICATE OF SERVICE**

I, Lourine K. McDuffie, hereby certify that on September 14, 2004, have caused a copy of the attached, *List of Exhibits that may be displayed or otherwise referred to during Complaint Counsel's Technology Presentation*, to be served upon the following persons:

by hand delivery to:

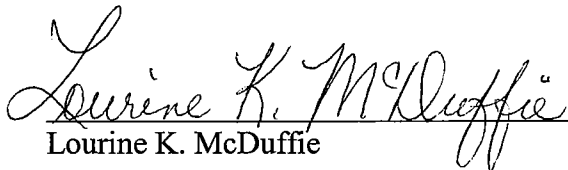
The Commissioners  
U.S. Federal Trade Commission  
Via Office of the Secretary, Room H-159  
Federal Trade Commission  
600 Pennsylvania Ave., N.W.  
Washington, D.C. 20580

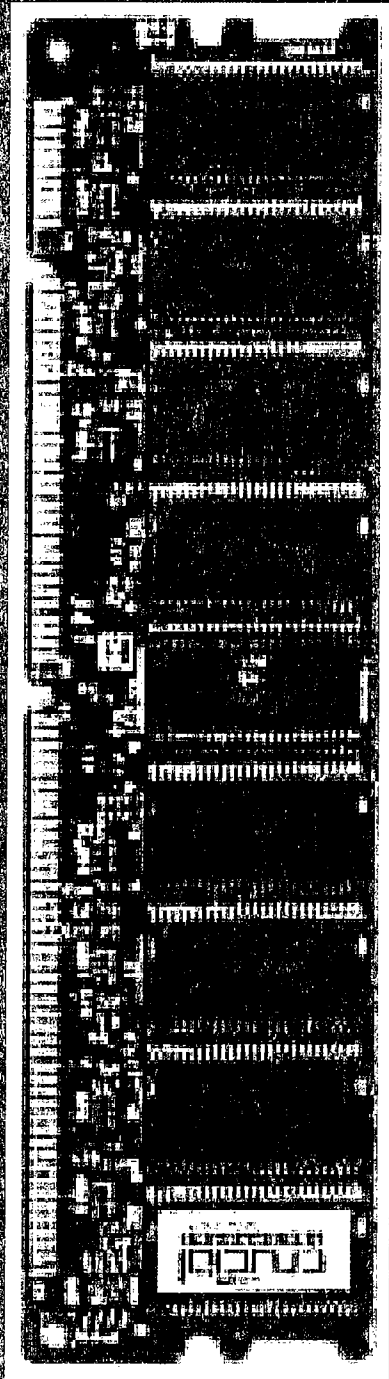
and by electronic transmission and overnight courier to:

A. Douglas Melamed, Esq.  
Wilmer Cutler Pickering LLP  
2445 M Street, N.W.  
Washington, DC 20037-1402

Steven M. Perry, Esq.  
Munger, Tolles & Olson LLP  
355 South Grand Avenue  
35<sup>th</sup> Floor  
Los Angeles, CA 90071

*Counsel for Rambus Incorporated*

  
Lourine K. McDuffie



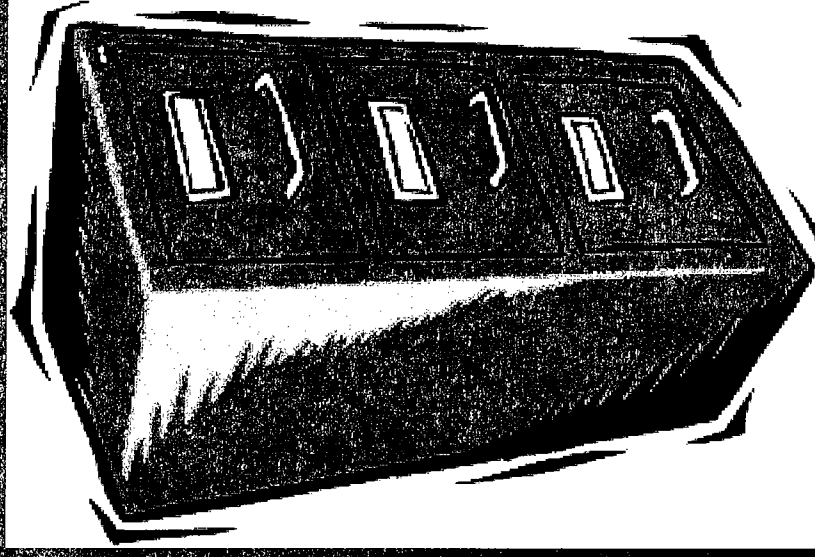
Similar to DX0001

# What Does Memory Do?

CPU →



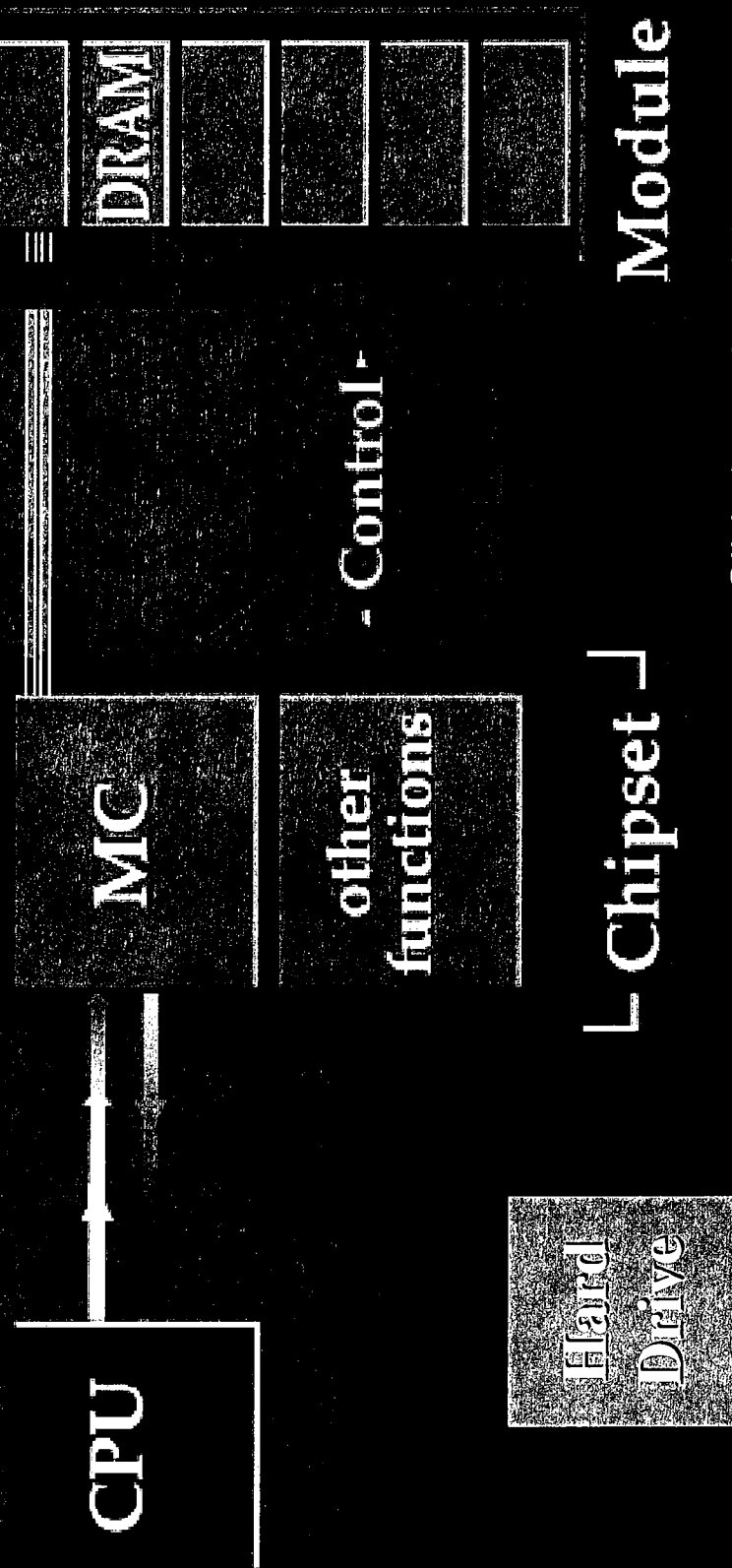
Memory ↗



↖ Hard Drive

# DRAM BASICS

## Interface



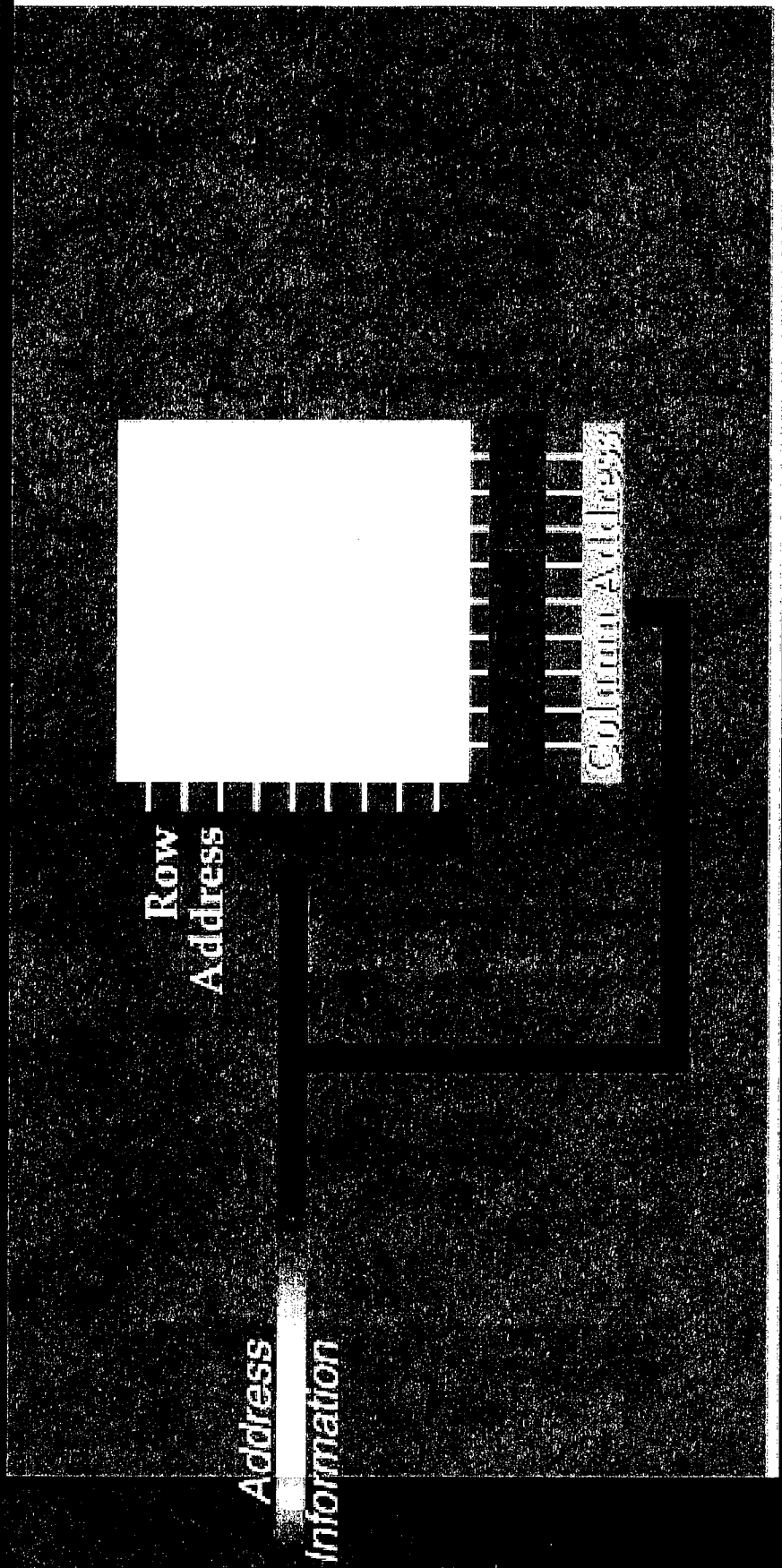
Slide based on DX0382-011

**B I N G O**



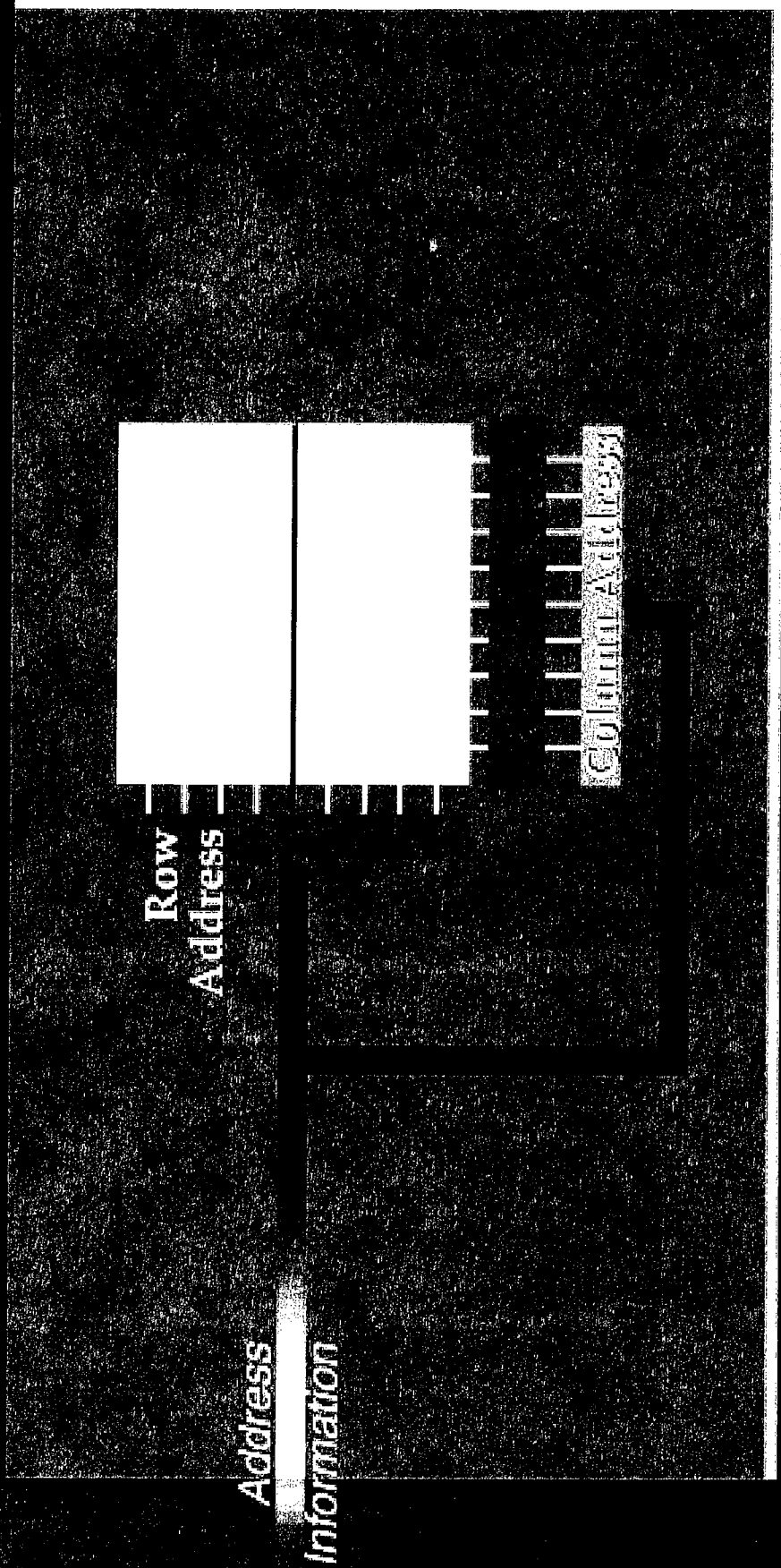

# DRAM

## Dynamic Random Access Memory



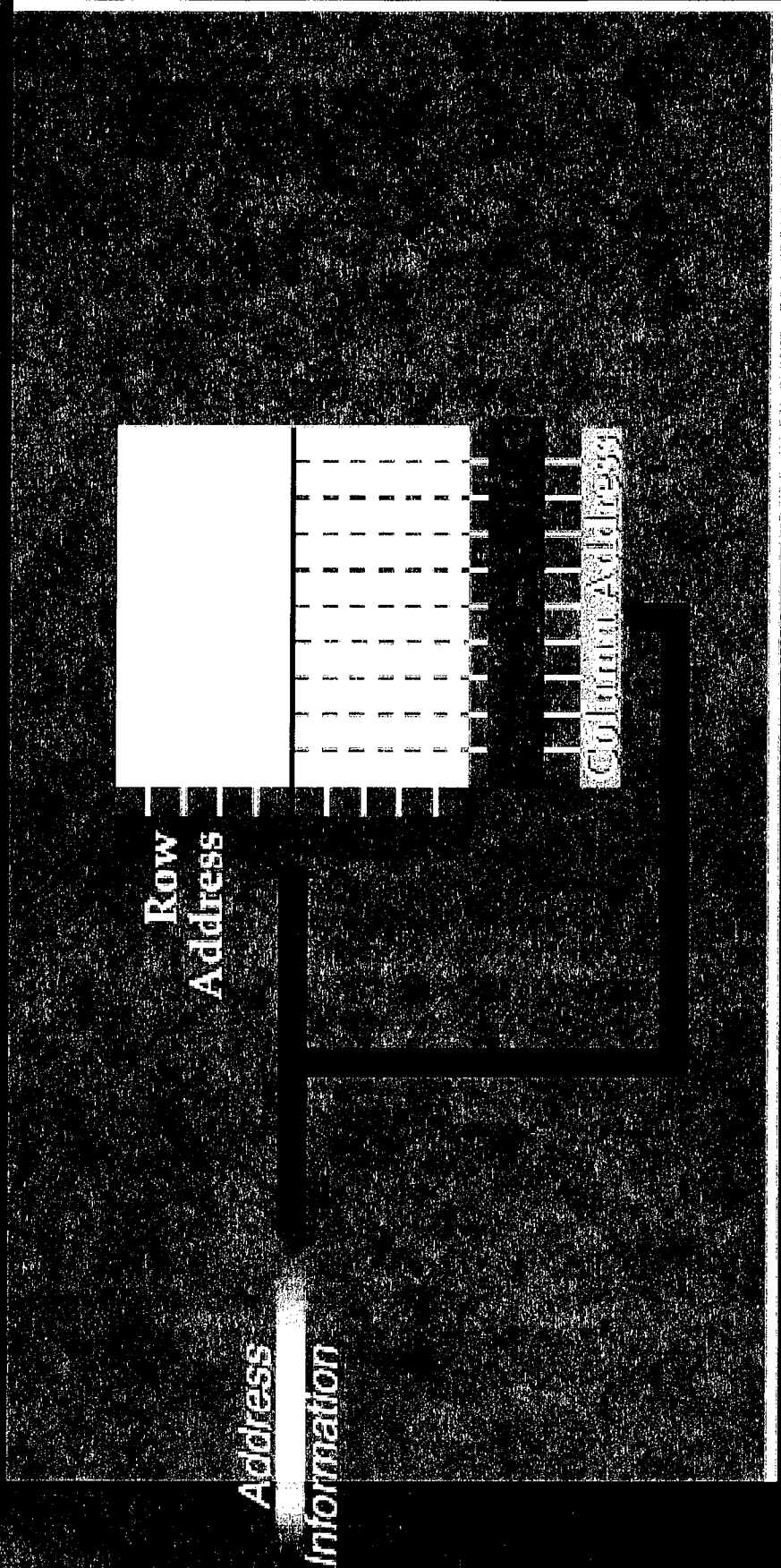
Slide based on DX0382-018

# DRAM Dynamic Random Access Memory



Slide based on DX0382-019

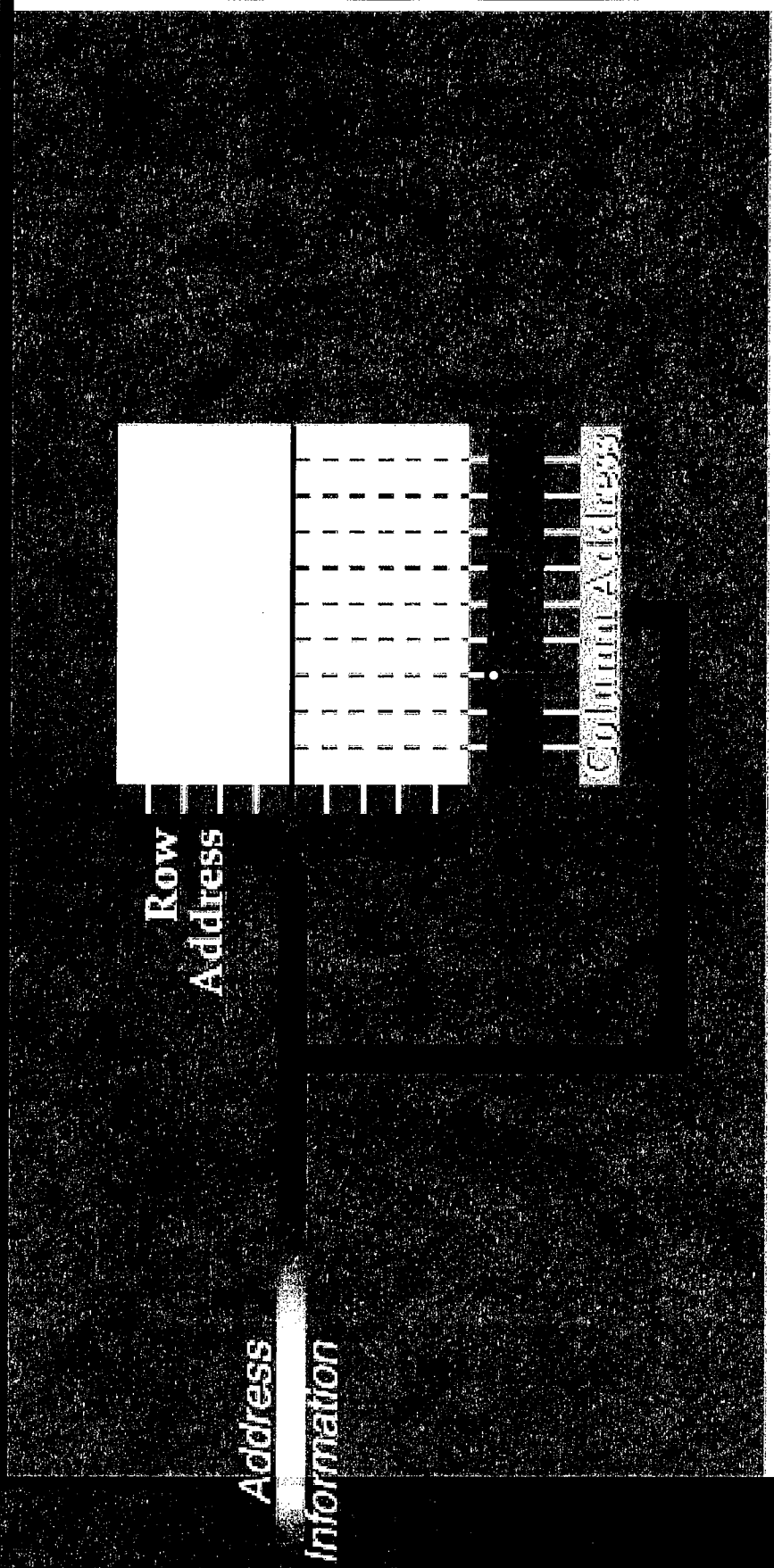
# DRAM Dynamic Random Access Memory



Slide based on DX0382-020

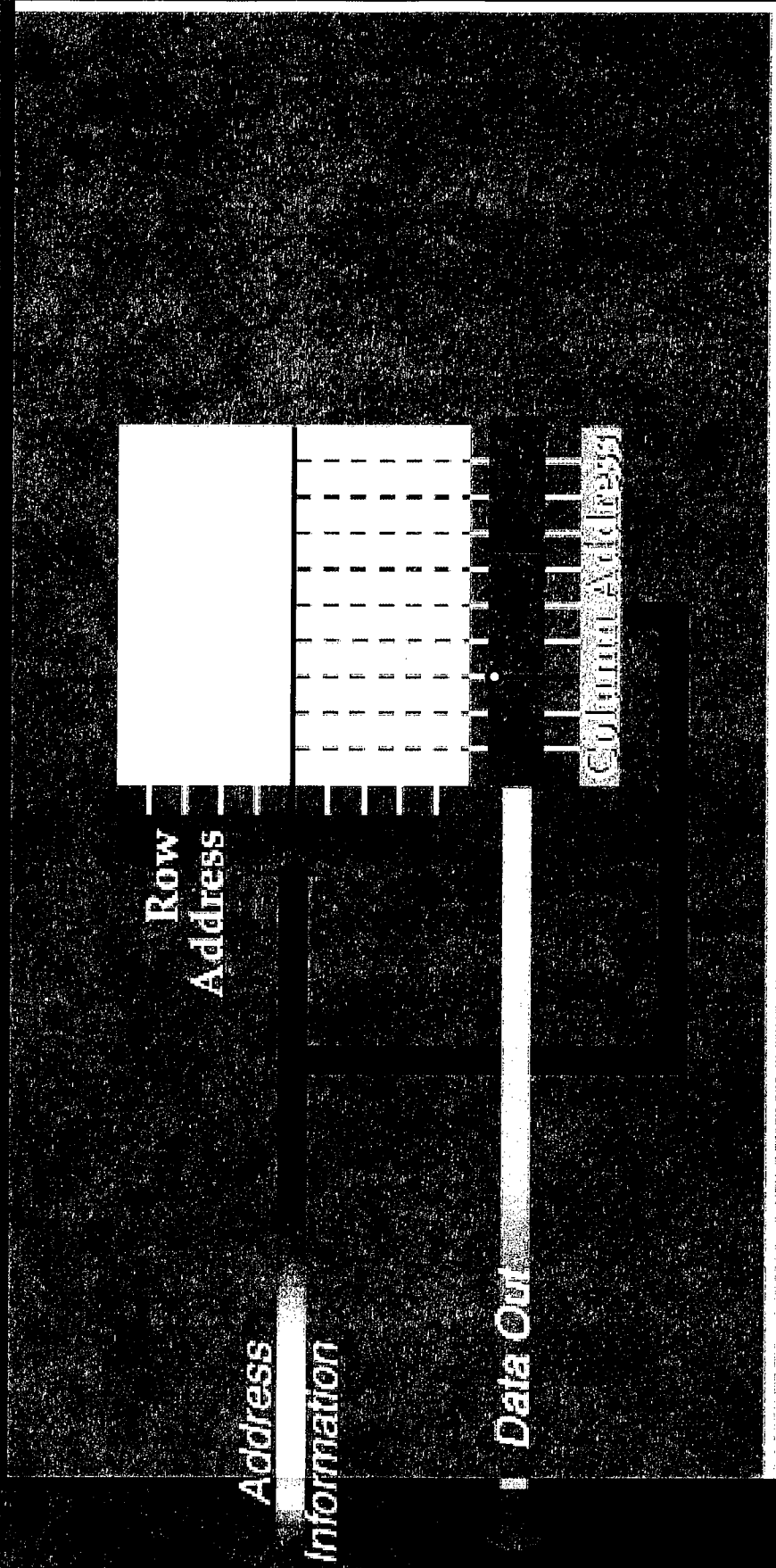
# DRAM

## Dynamic Random Access Memory



Slide based on DX0382-021

# DRAM Dynamic Random Access Memory



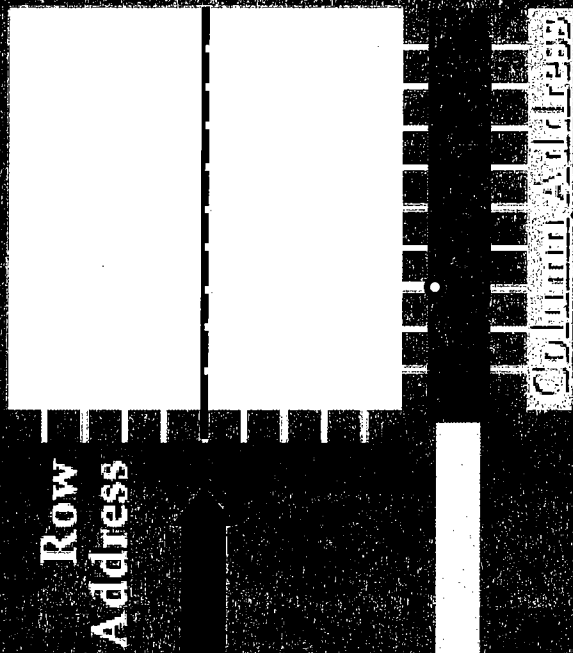
Slide based on DX0382-022

# DRAM Burst Length

Row  
Address

Column Address

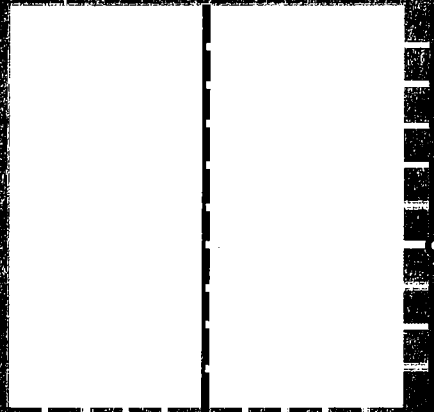
# DRAM Burst Length



Based on DX0382-042

# DRAM Burst Length

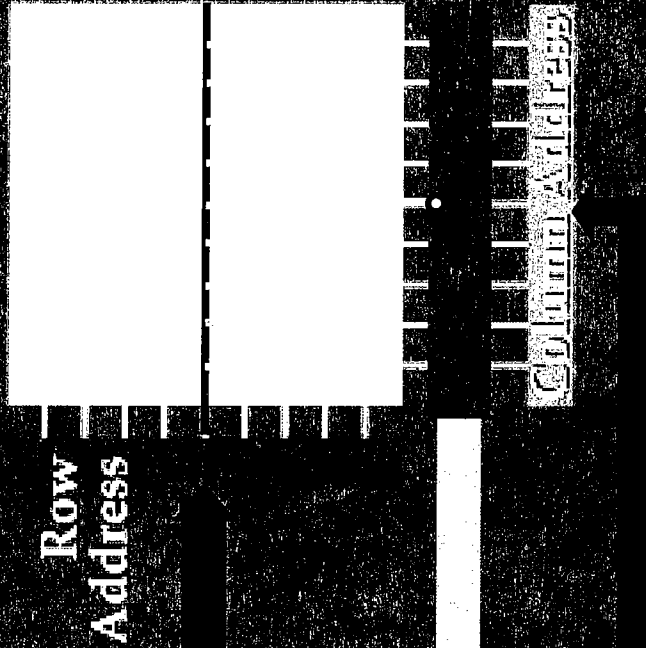
Row  
Address



Column  
Address



# DRAM Burst Length



Based on DX0382-042

# Synchronous DRAM

WIDE BUS - SDR

Clock -

Control 4 lines

12 Address lines (A0 - A11)

16 Data lines (DQ0 - DQ15)

MC

DRAM

# Synchronous DRAM

WIDE BUS - DDR

Clock -

Control Lines

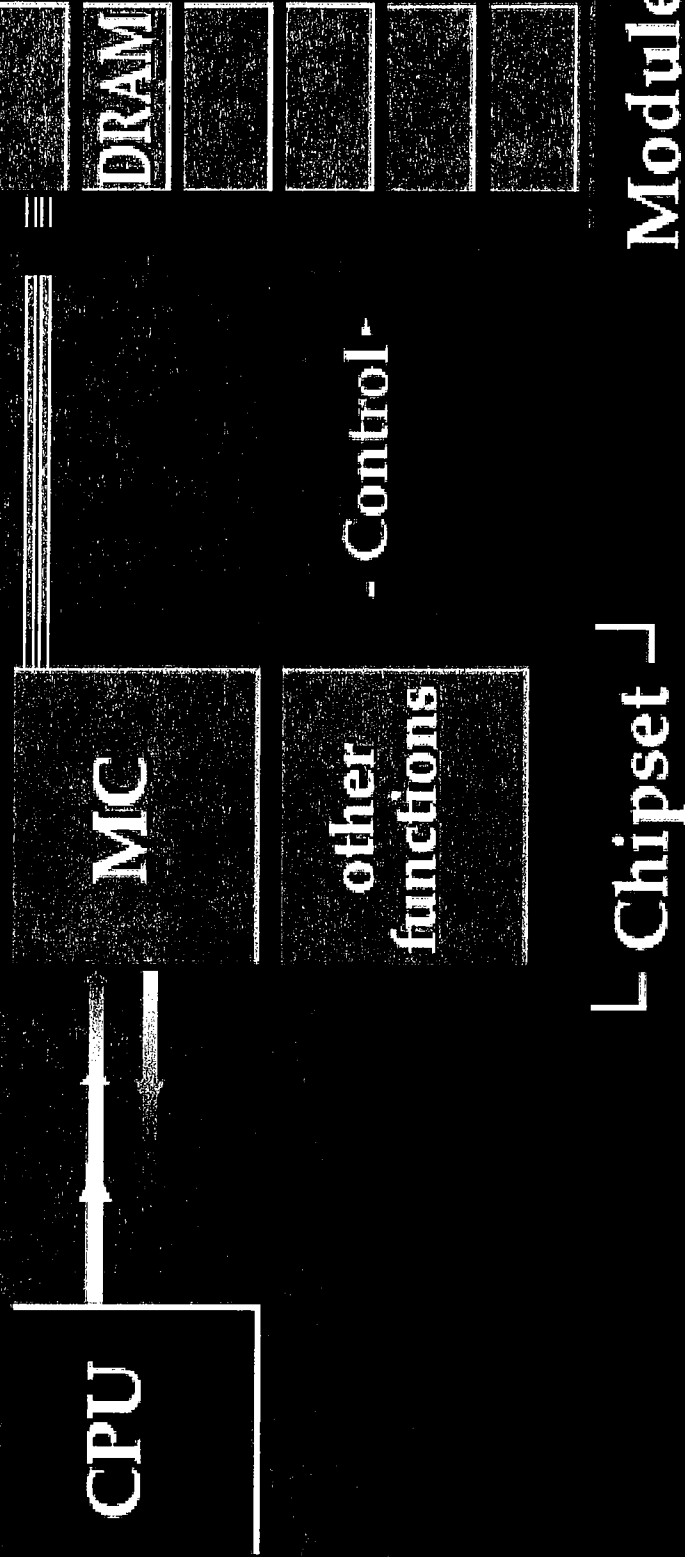
12 Address lines (A0 - A11)

16 Data lines (DQ0 - DQ15)

DQS#

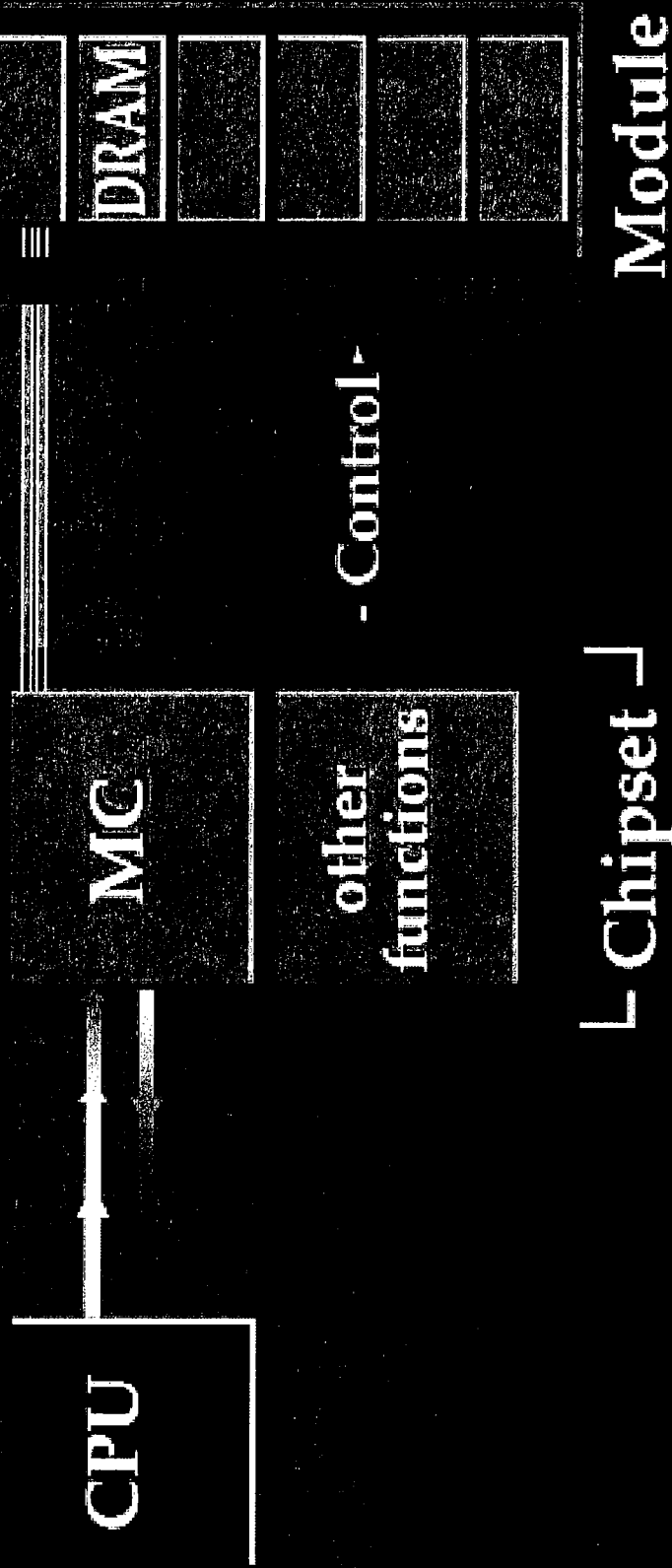
DQS# Data Strobe

# DRAM BASICS Interface



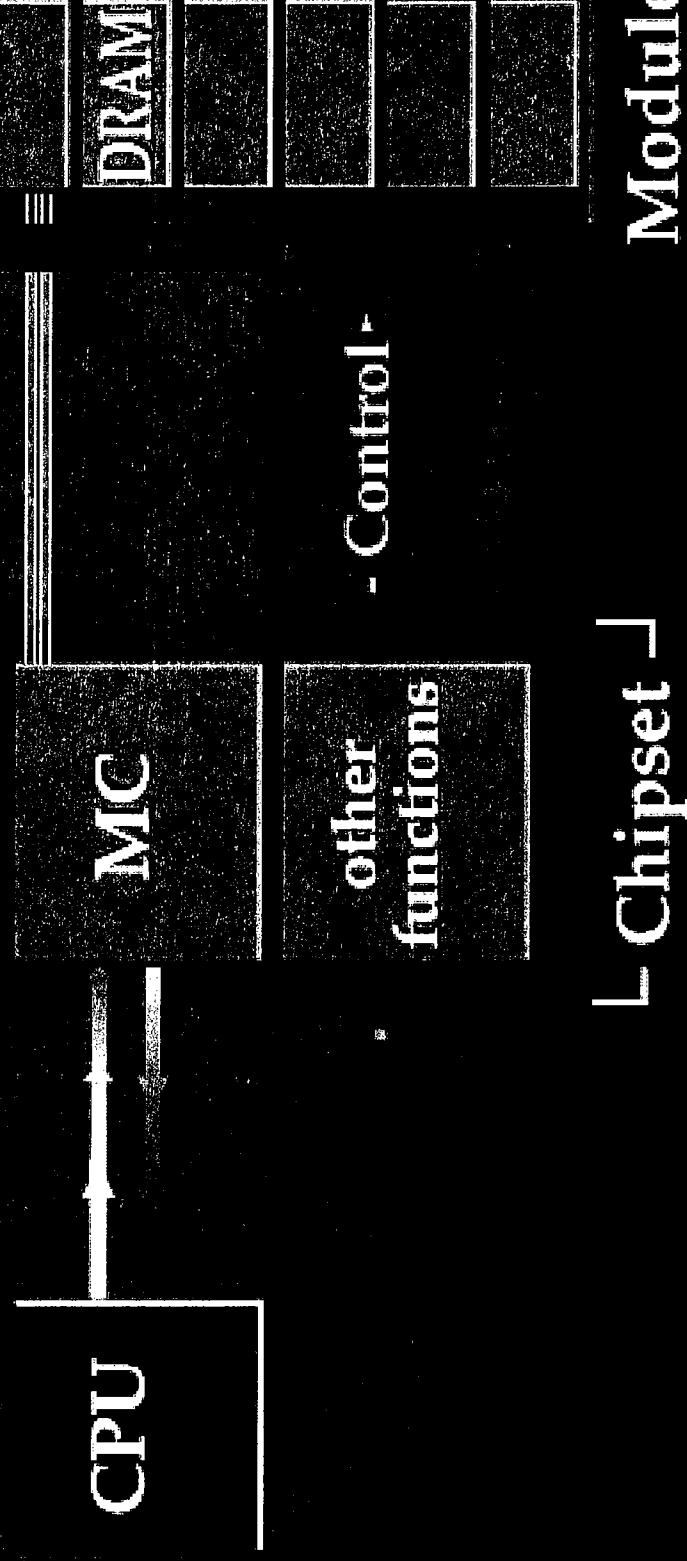
Slide based on DX0382-009

# DRAM BASICS Interface



Slide based on DX0382-010

# DRAM BASICS Interface



Slide based on DX0382-011

5

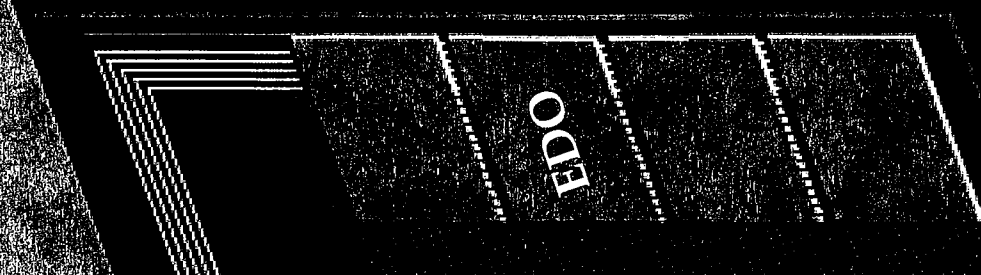
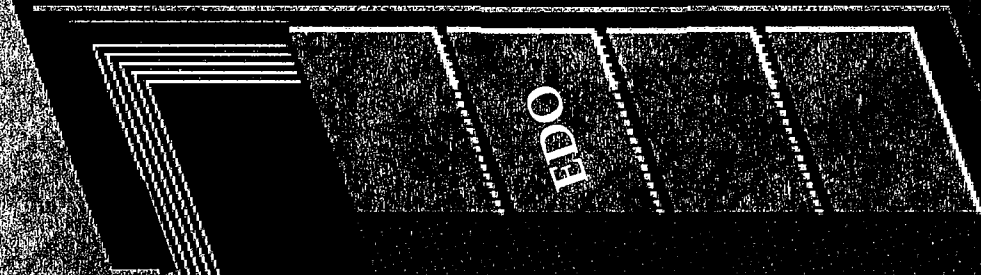
Control

15

Address

MC

64 Data



Slide based on DX0382-031

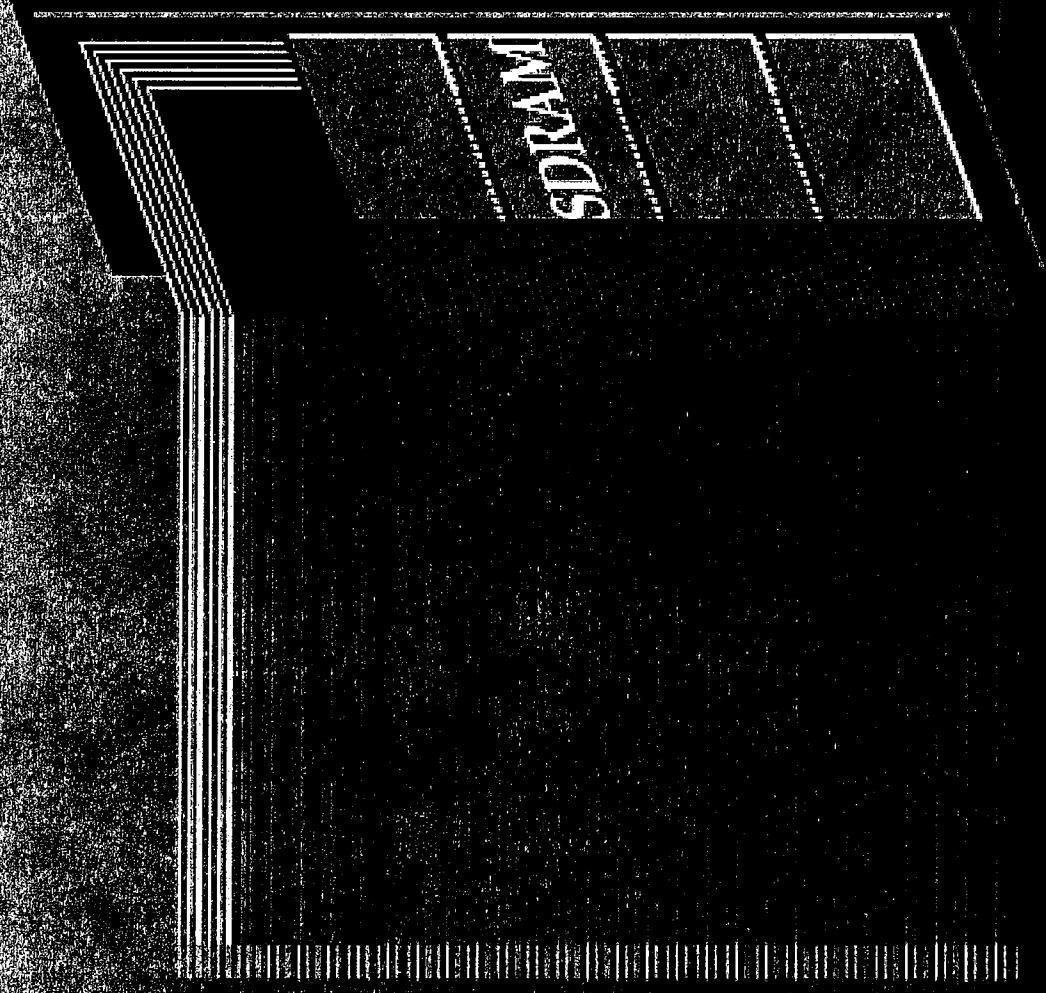
Ck

5  
Control

15  
Address

MC

64 Data



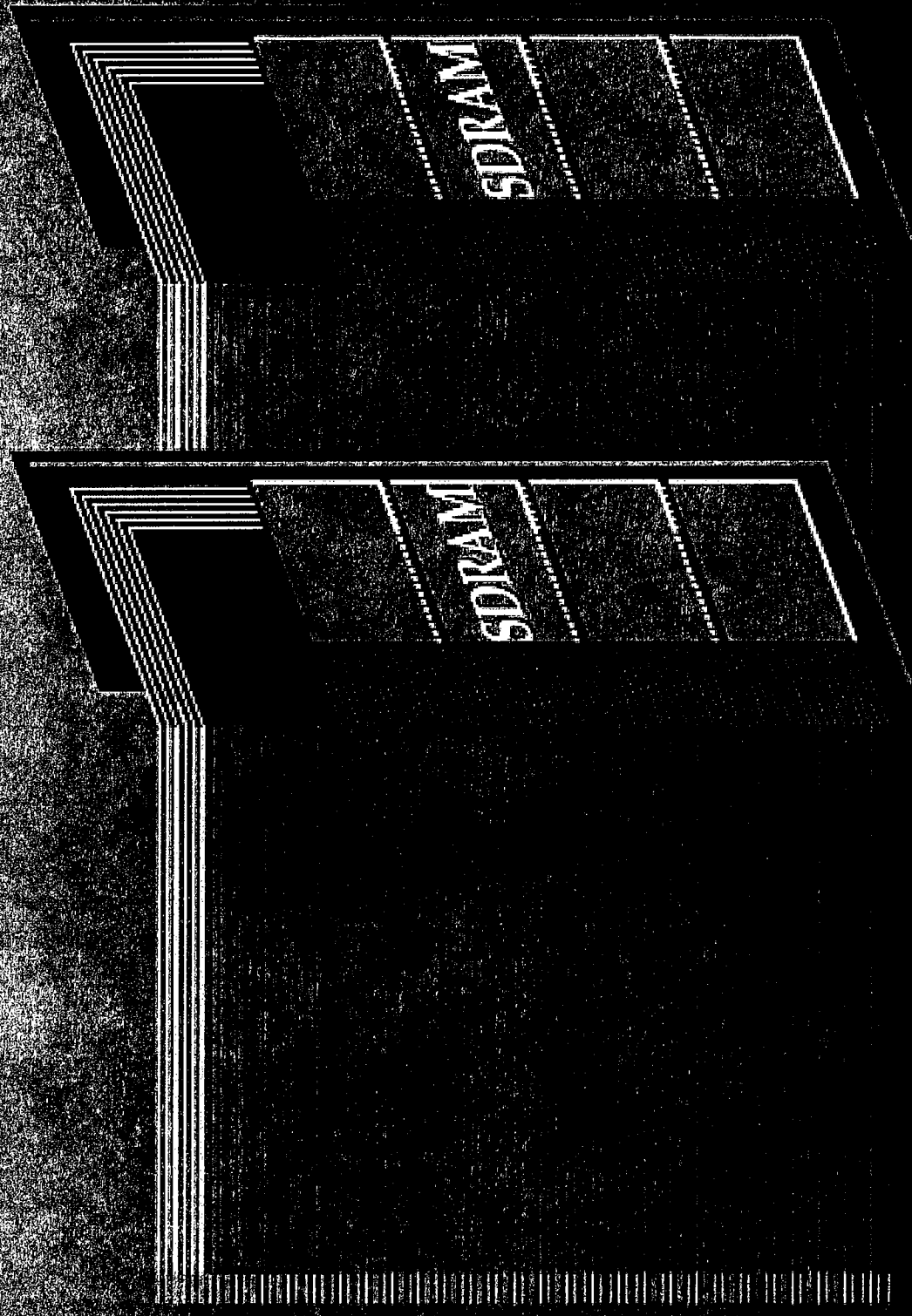
Slide based on DX0382-031



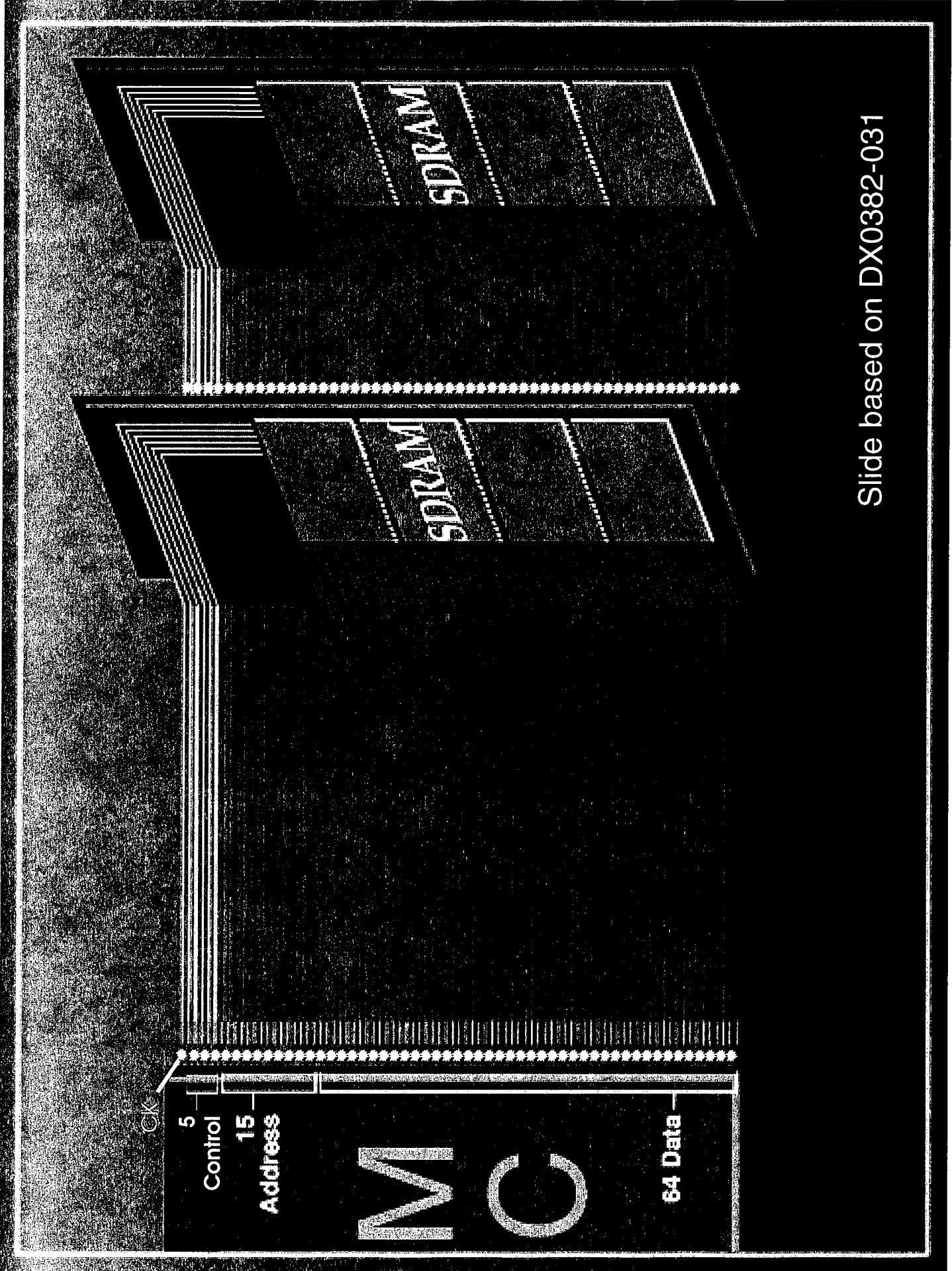
15  
Address

MC

64 Data

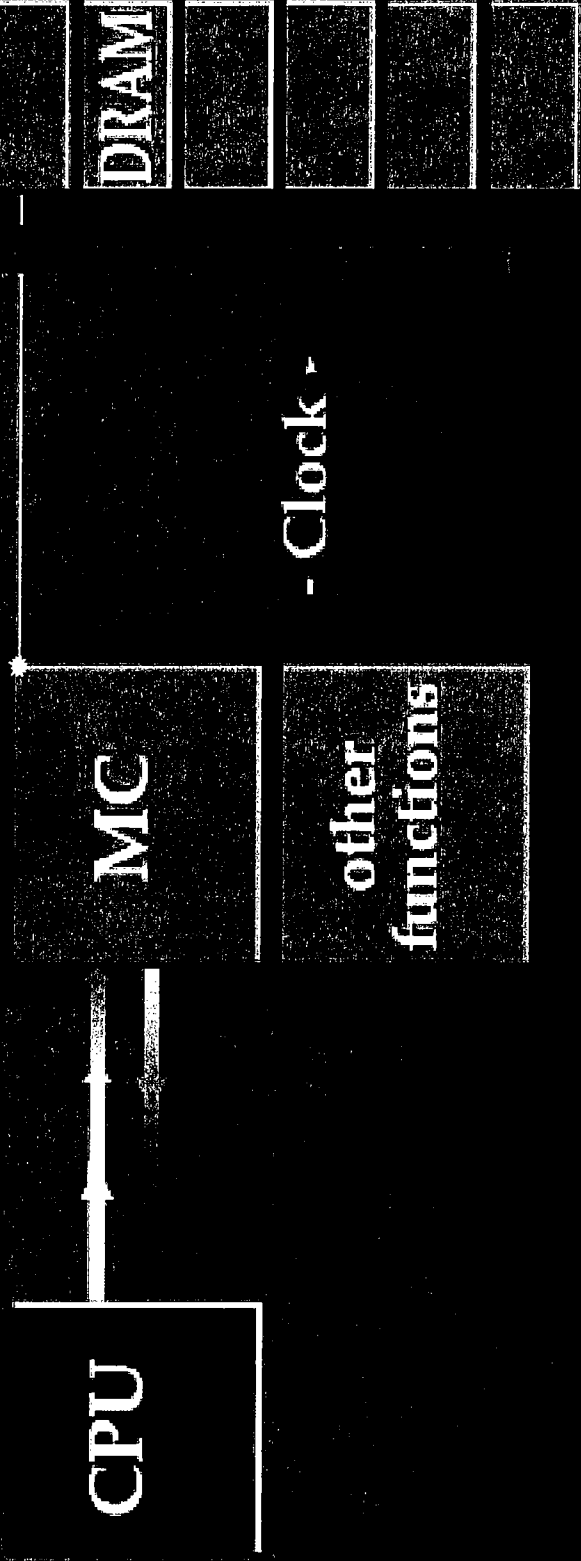


Slide based on DX0382-031



Slide based on DX0382-031

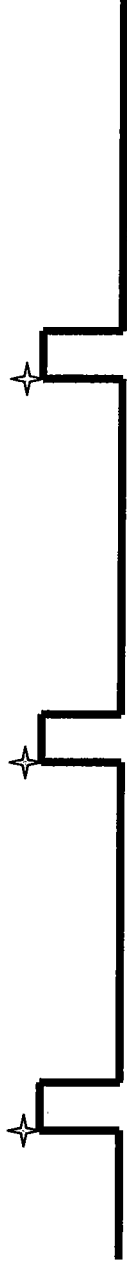
# DRAM BASICS Interface



└ Chipset ─

Module

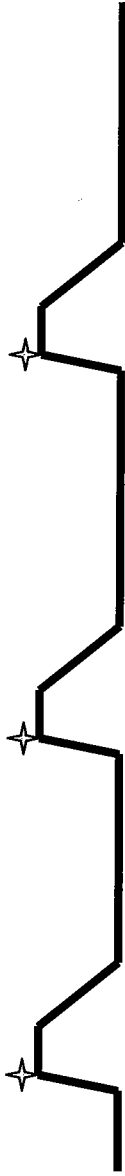
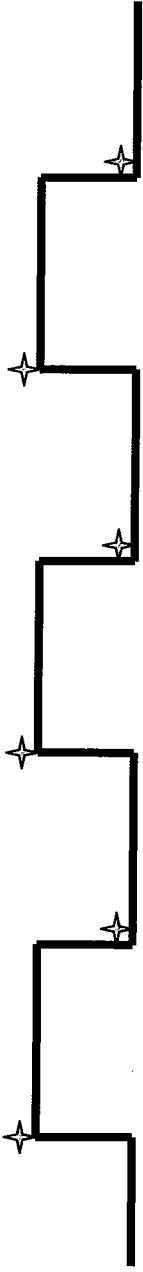
Slide based on DX0382-008



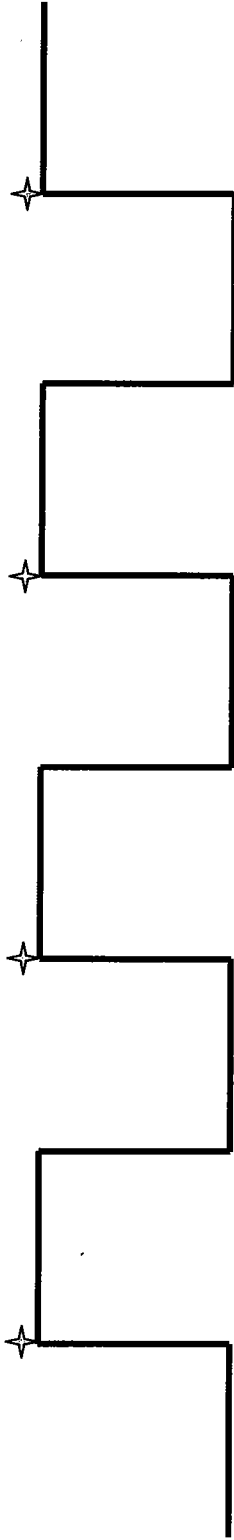
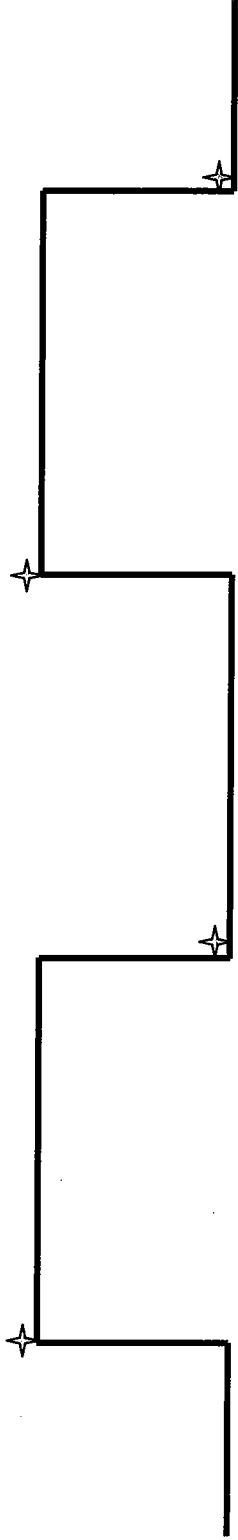
Slide based on DX0358



Slide based on DX0358



Slide based on DX0358



Slide based on DX0358

# Methods to Specify Latency

- Use one or more fixed latencies
- Use a fuse to set latency
- Use a pin to set latency
- Specify latency in the read command
- Scale latency with the clock frequency
- Continue to use Asynchronous DRAMs



# Methods to Specify Burst Length

- Use one or more fixed burst lengths
- Use a fuse to set burst length
- Use a pin to set burst length
- Specify burst length in the read command
- Use fixed burst length with a burst terminate command
- Use CAS pulse to control data output

# Methods to Accelerate Data Transfer

- Single Edge Clock

  - Faster Clock

  - Clock Splitter

- Interleave Memory Access/Banks

  - On DRAM

- Simultaneous Bi-directional I/O Drivers

From DX0088, DX0060, CX0371

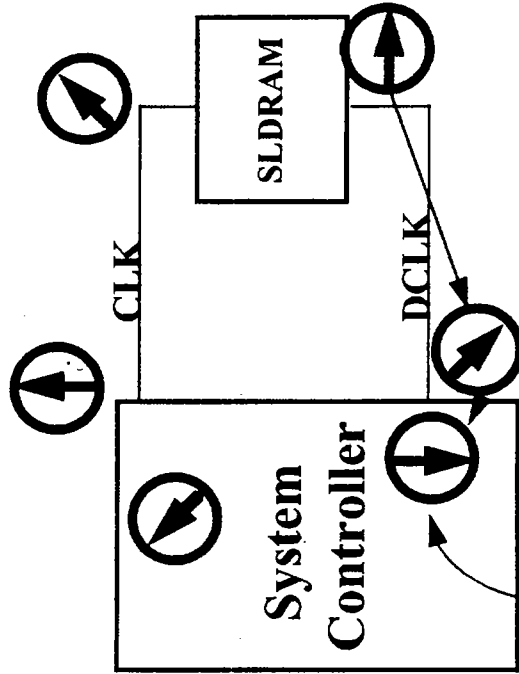
# Methods of Synchronizing Data

- PLL/DLL on chip
- PLL/DLL on module
- PLL/DLL on controller

Data Storage

# Mini System Block Diagram

Without Vernier



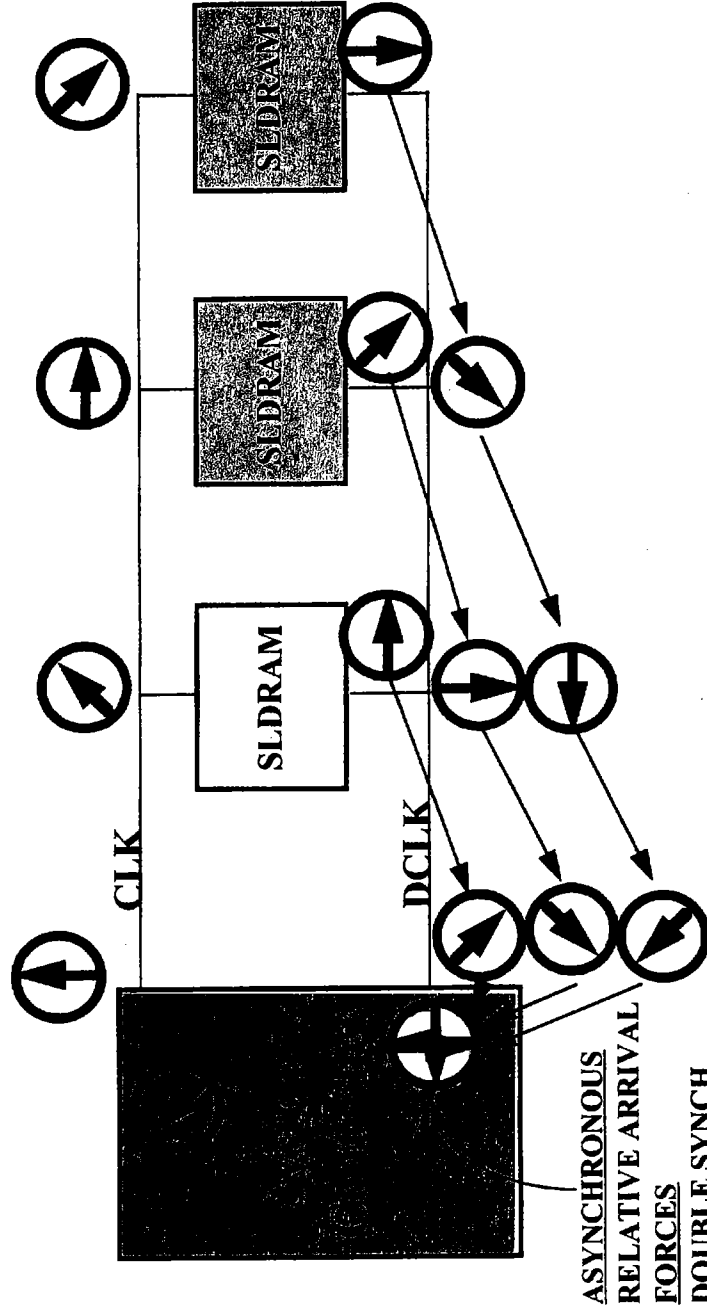
**ASYNCHRONOUS RELATIVE ARRIVAL COULD FORCE DOUBLE SYNC DELAY INSIDE CONTROLLER**

Note: In the minimum system, arrival time could be detected and adjusted inside the controller to a max delay of one DCLK with an internal vernier, but would most likely require the DCLK to run continuously. For systems with more than one memory device, such adjustment would not be feasible.

Note: Synchronizing inside controller would typically be to controller clock that would likely be 1/2 or 1/4 memory clock speed, so the synchronizing delay would be very costly for system performance

# Simple System Block Diagram

Without Vernier

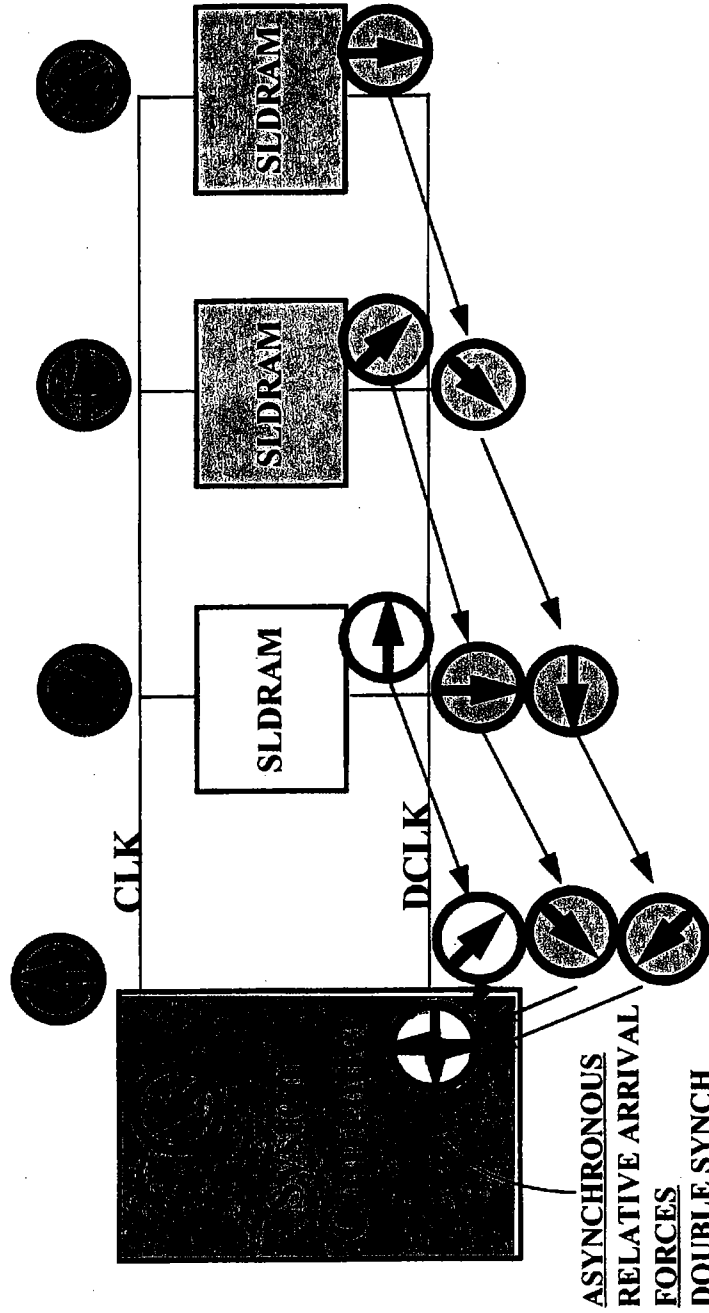


ASYNCHRONOUS  
 RELATIVE ARRIVAL  
 FORCES  
 DOUBLE SYNCH  
 DELAY INSIDE  
 CONTROLLER

Note: Synchronizing inside controller would typically be to controller clock that would likely be 1/2 or 1/4 memory clock speed, so the synchronizing delay would be very costly for system performance

# Simple System Block Diagram

Without Vernier

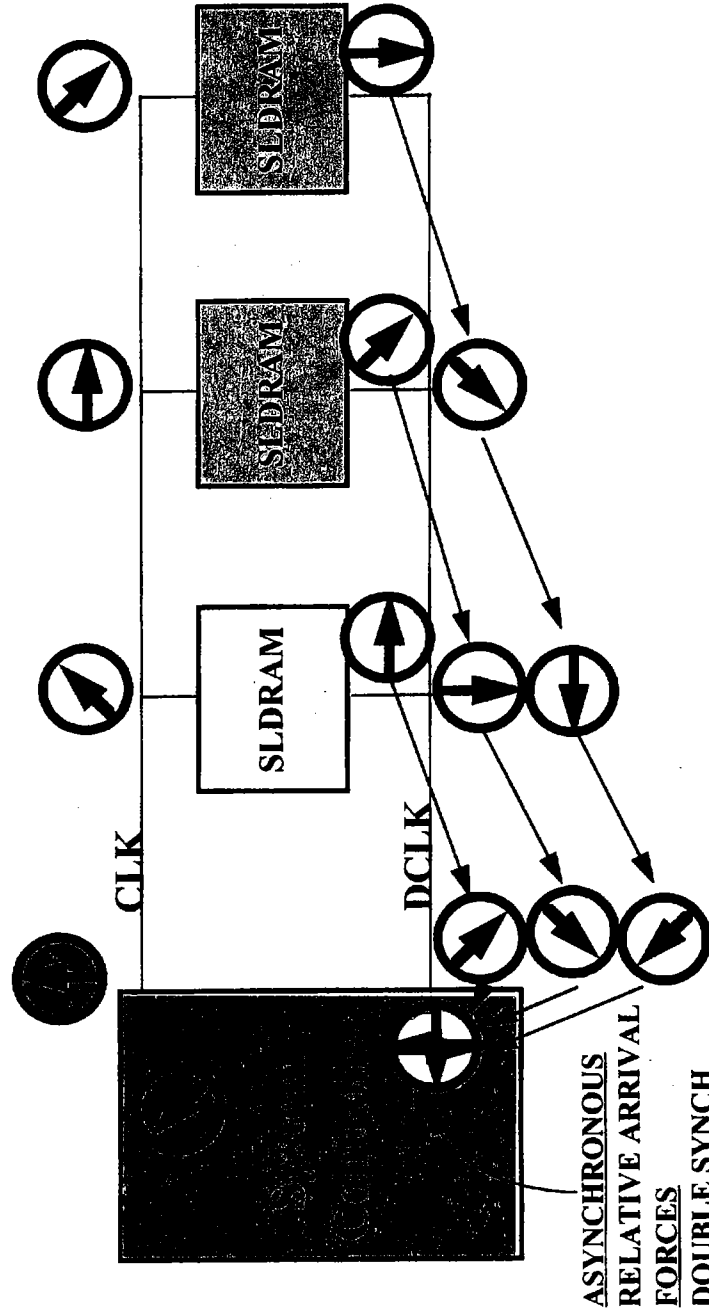


**ASYNCHRONOUS RELATIVE ARRIVAL FORCES DOUBLE SYNCH DELAY INSIDE CONTROLLER**

Note: Synchronizing inside controller would typically be to controller clock that would likely be 1/2 or 1/4 memory clock speed, so the synchronizing delay would be very costly for system performance

# Simple System Block Diagram

Without Vernier

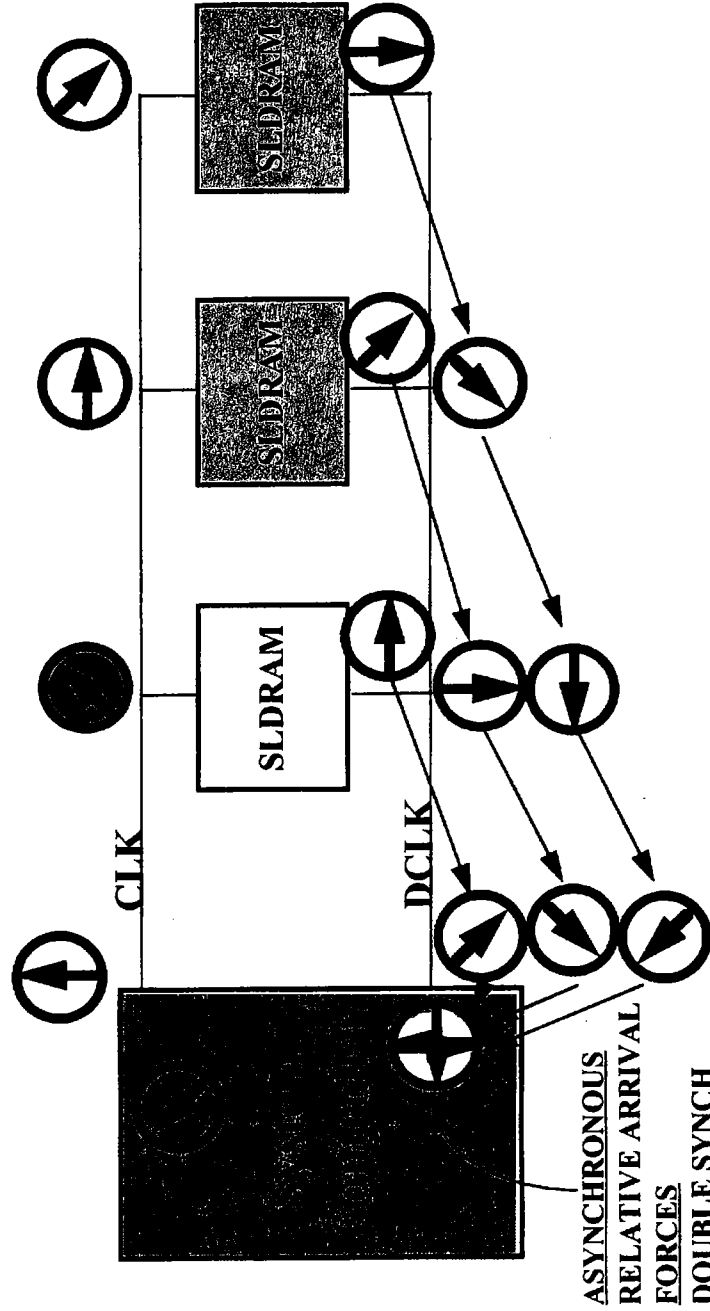


ASYNCHRONOUS  
RELATIVE ARRIVAL  
FORCES  
DOUBLE SYNC  
DELAY INSIDE  
CONTROLLER

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# Simple System Block Diagram

Without Vernier



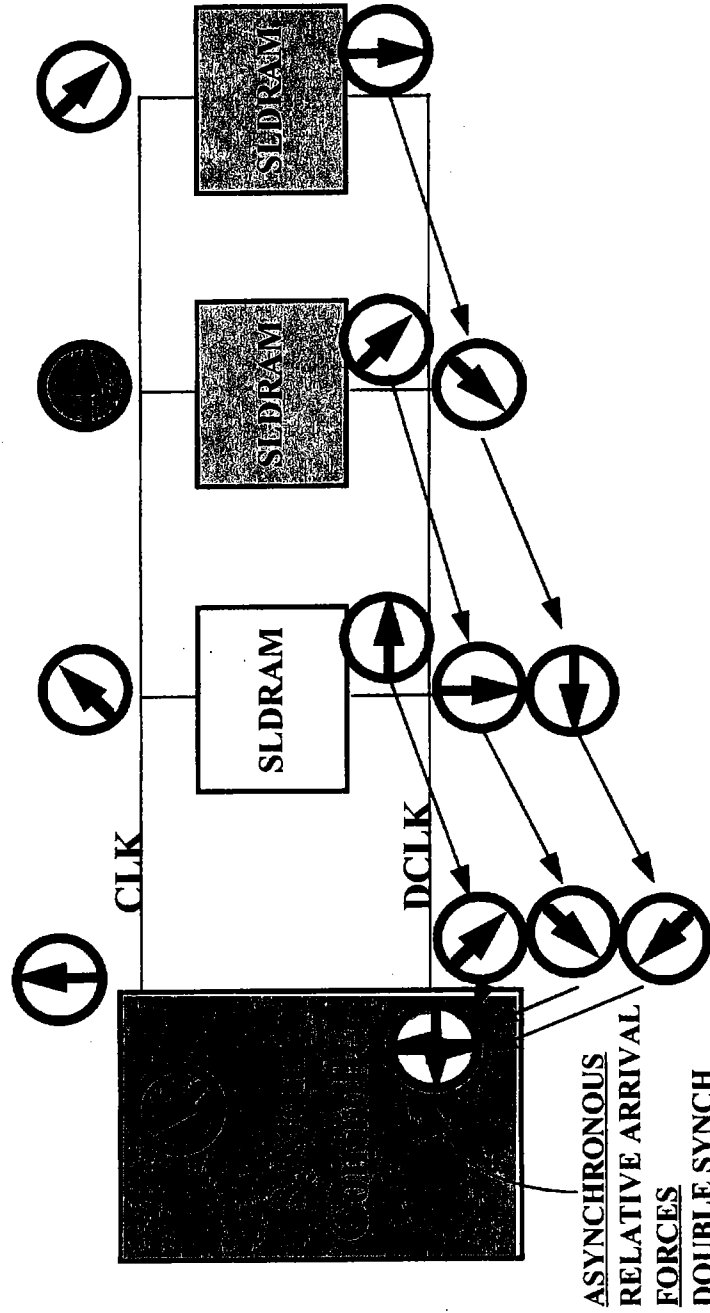
**ASYNCHRONOUS RELATIVE ARRIVAL FORCES**  
**DOUBLE SYNCH DELAY INSIDE CONTROLLER**

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# Simple System Block Diagram

Without Vernier

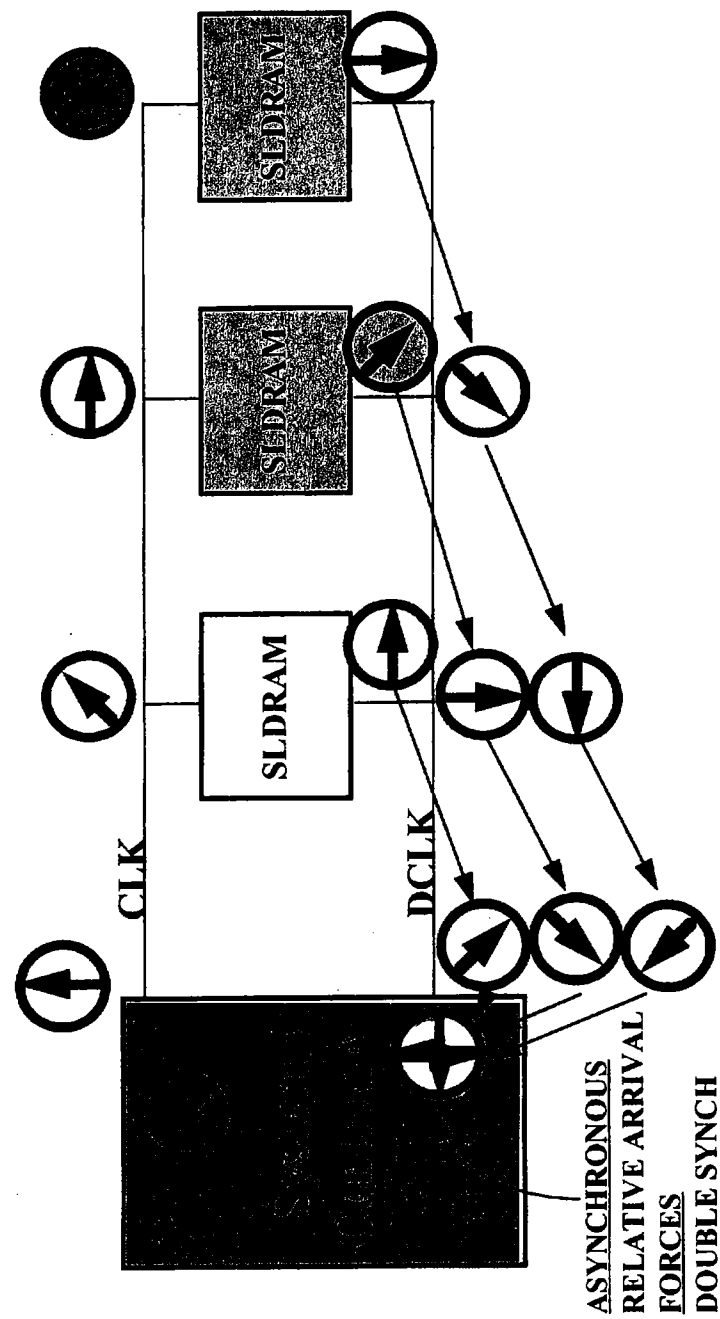


**ASYNCHRONOUS**  
**RELATIVE ARRIVAL**  
**FORCES**  
**DOUBLE SYNCH**  
**DELAY INSIDE**  
**CONTROLLER**

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# Simple System Block Diagram

Without Vernier

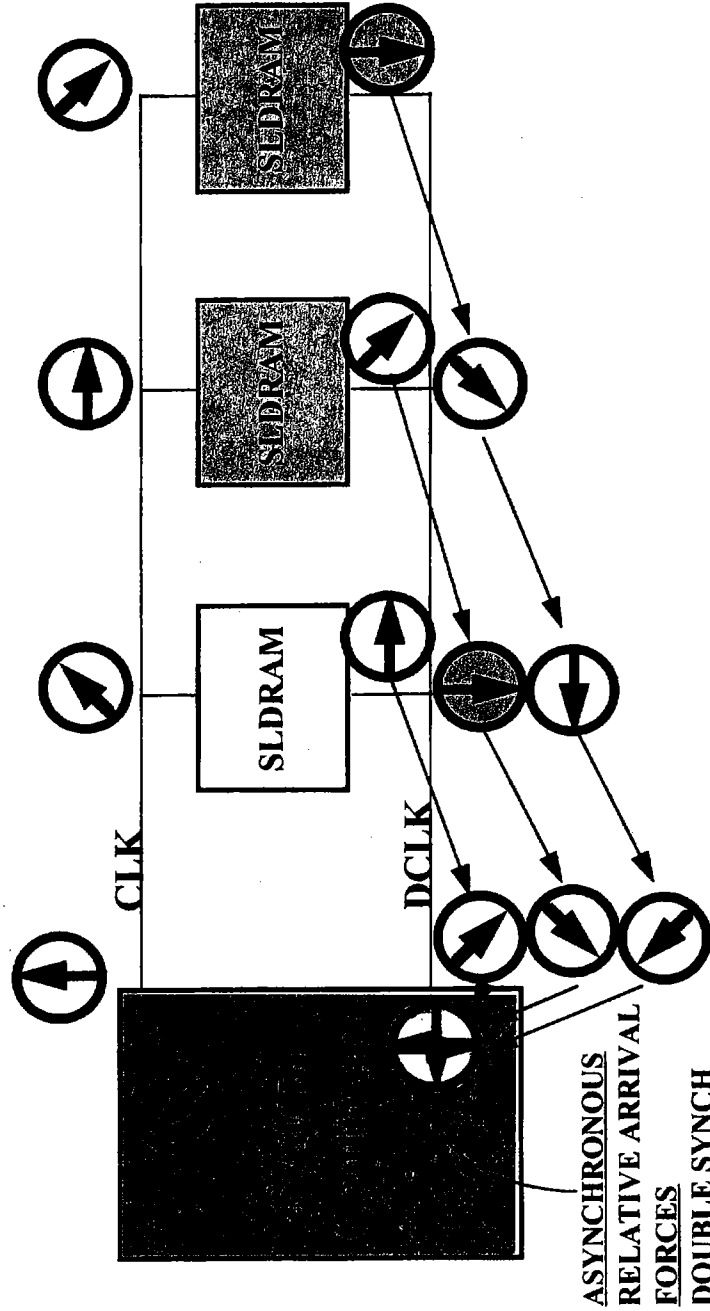


**ASYNCHRONOUS  
RELATIVE ARRIVAL  
FORCES  
DOUBLE SYNC  
DELAY INSIDE  
CONTROLLER**

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# Simple System Block Diagram

Without Vernier

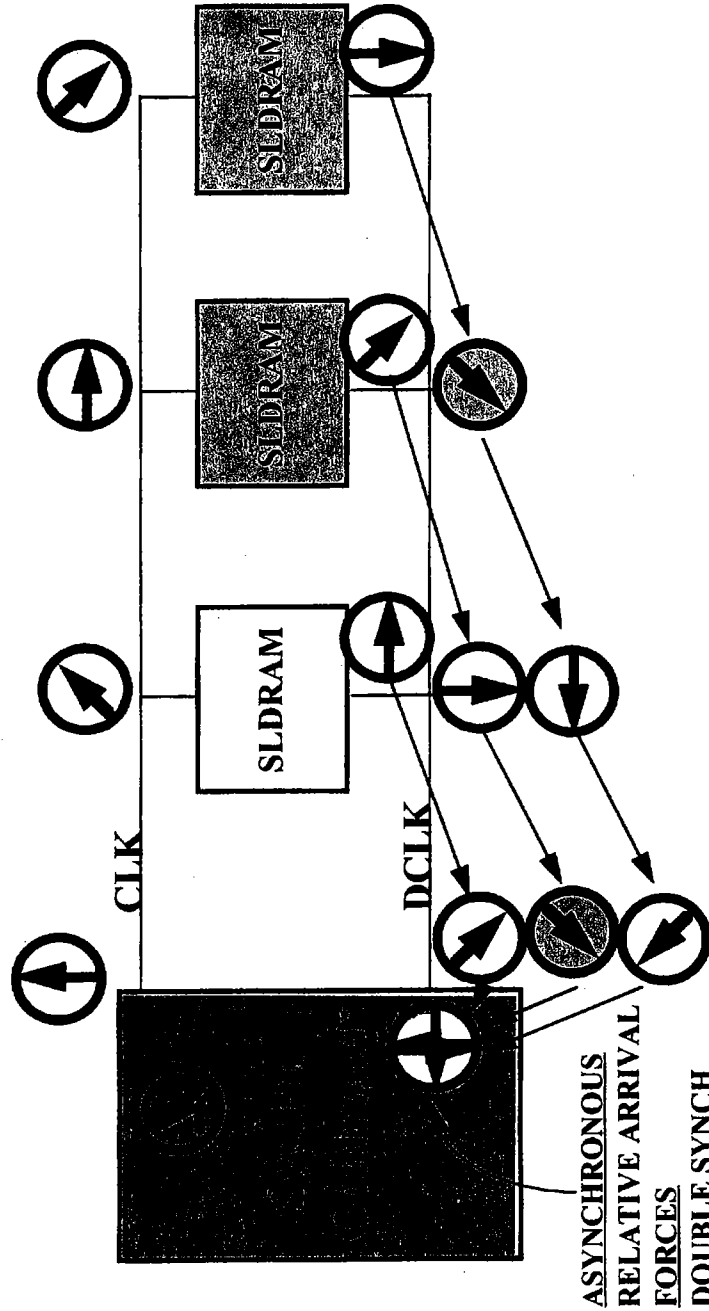


**ASYNCHRONOUS  
RELATIVE ARRIVAL  
FORCES  
DOUBLE SYNCH  
DELAY INSIDE  
CONTROLLER**

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# Simple System Block Diagram

Without Vernier

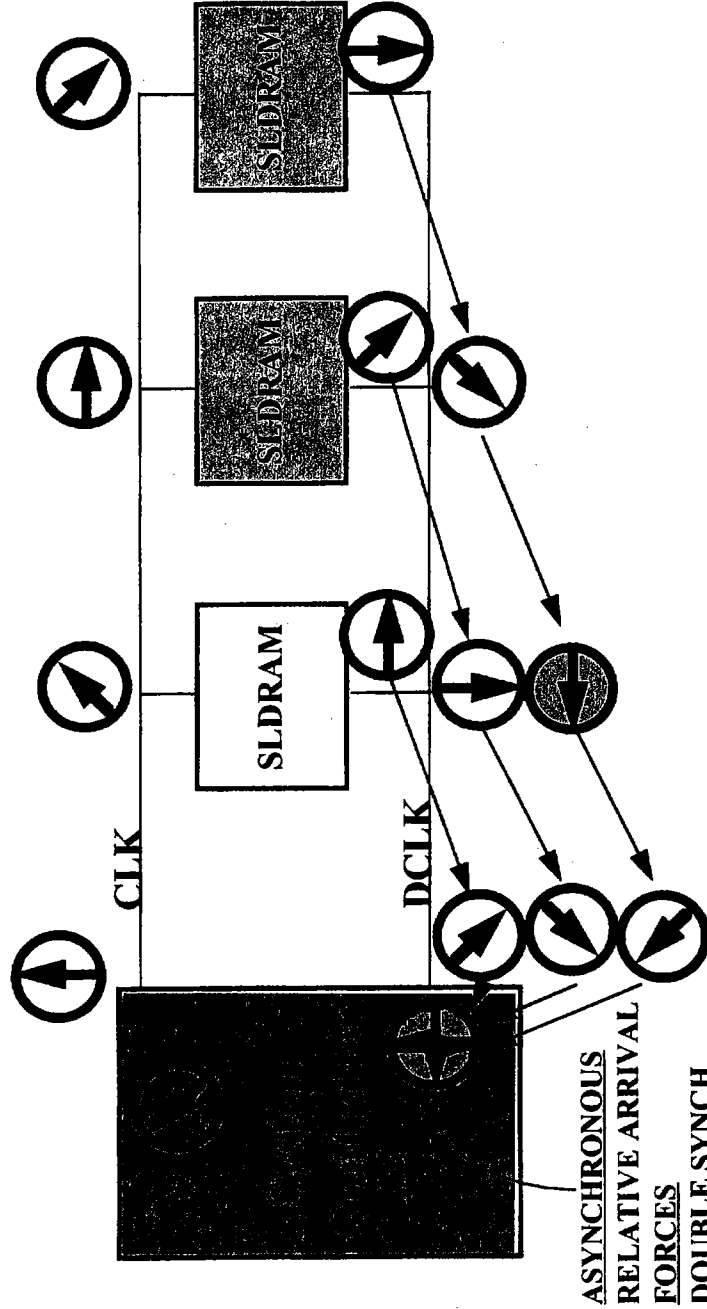


ASYNCHRONOUS  
 RELATIVE ARRIVAL  
 FORCES  
 DOUBLE SYNCH  
 DELAY INSIDE  
 CONTROLLER

Note: Synchronizing inside controller would typically be to controller clock that would likely be 1/2 or 1/4 memory clock speed, so the synchronizing delay would be very costly for system performance

# Simple System Block Diagram

Without Vernier

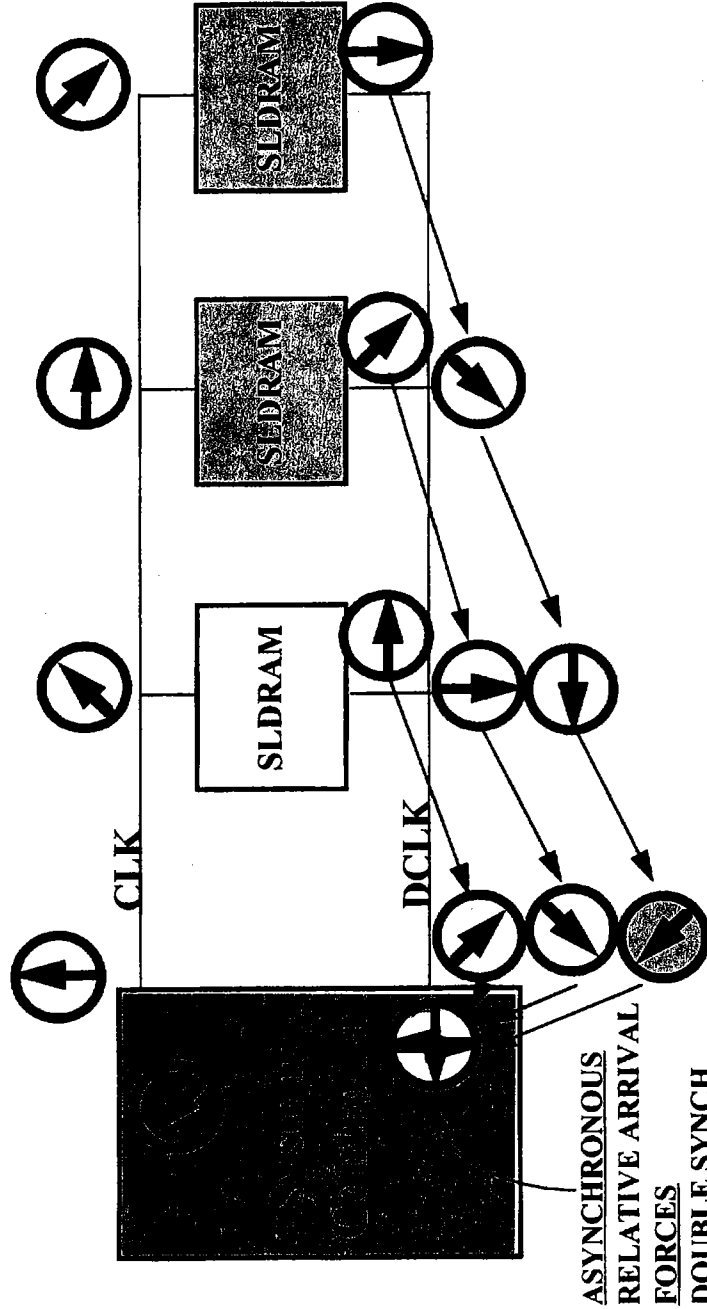


**ASYNCHRONOUS  
RELATIVE ARRIVAL  
FORCES  
DOUBLE SYNCH  
DELAY INSIDE  
CONTROLLER**

**Note:** Synchronizing inside controller would typically be to controller clock that would likely be 1/2 or 1/4 memory clock speed, so the synchronizing delay would be very costly for system performance

# Simple System Block Diagram

Without Vernier

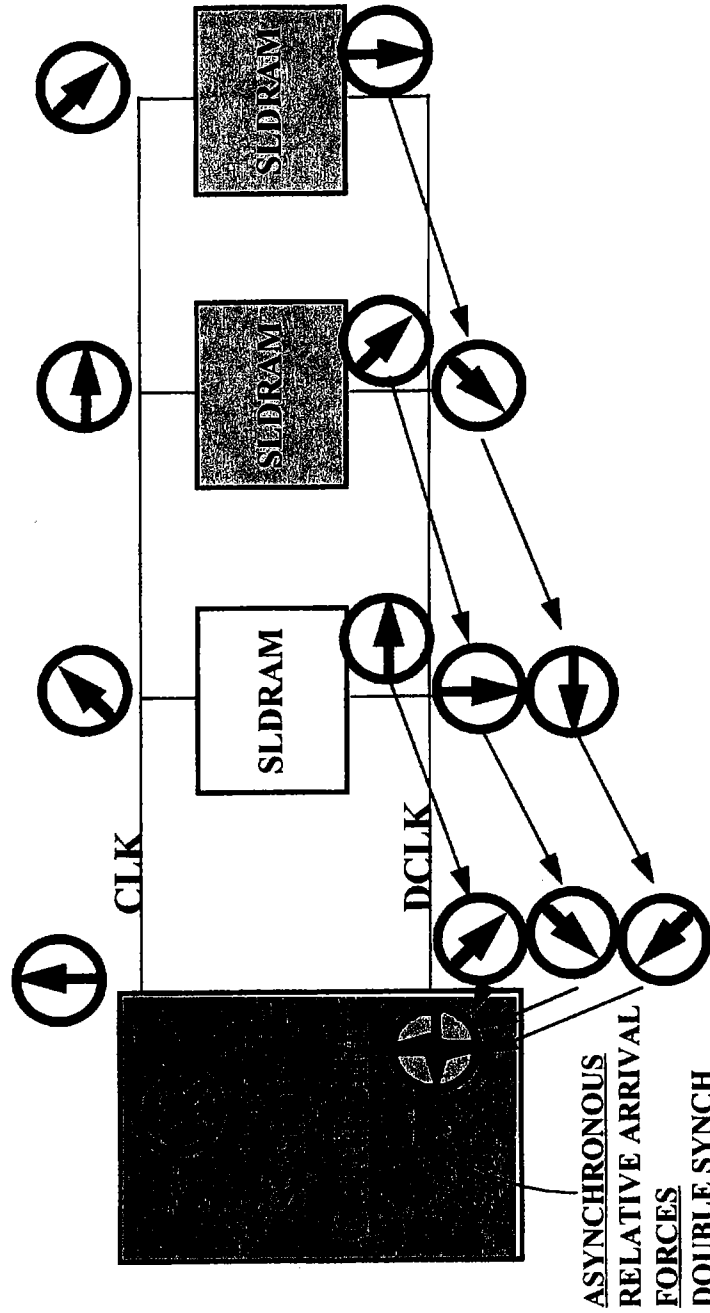


**ASYNCHRONOUS RELATIVE ARRIVAL FORCES**  
**DOUBLE SYNCH DELAY INSIDE CONTROLLER**  
**ASYNCHRONOUS RELATIVE ARRIVAL FORCES**

Note: Synchronizing inside controller would typically be to controller clock that would likely be 1/2 or 1/4 memory clock speed, so the synchronizing delay would be very costly for system performance

# Simple System Block Diagram

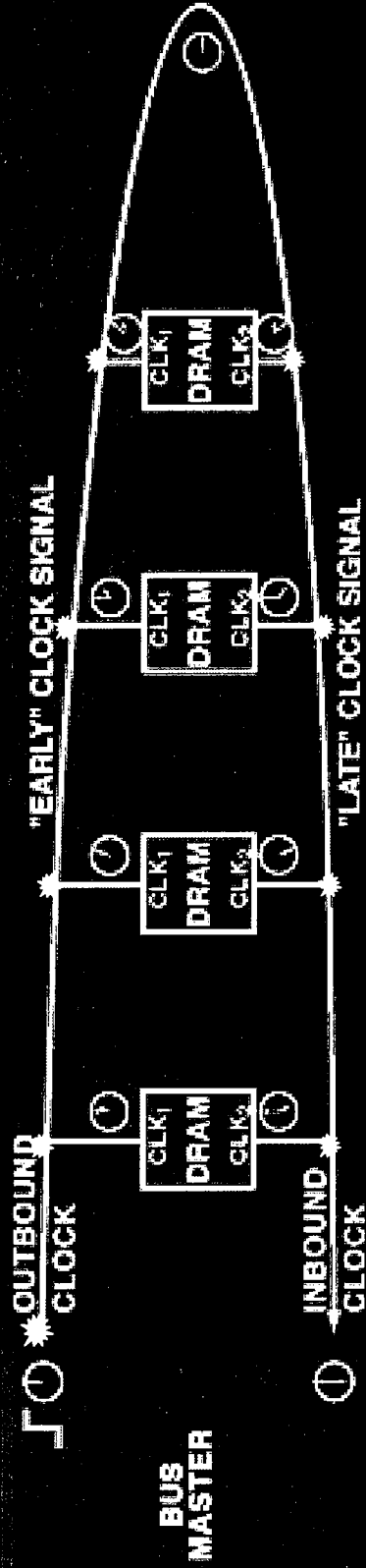
Without Vernier



ASYNCHRONOUS  
RELATIVE ARRIVAL  
FORCES  
DOUBLE SYNCH  
DELAY INSIDE  
CONTROLLER

Note: Synchronizing inside controller would typically be to controller clock that would likely be 1/2 or 1/4 memory clock speed, so the synchronizing delay would be very costly for system performance

# RAMBUS CLOCK SYNCHRONIZATION



Slide based on DX0382-051



# RDRAM

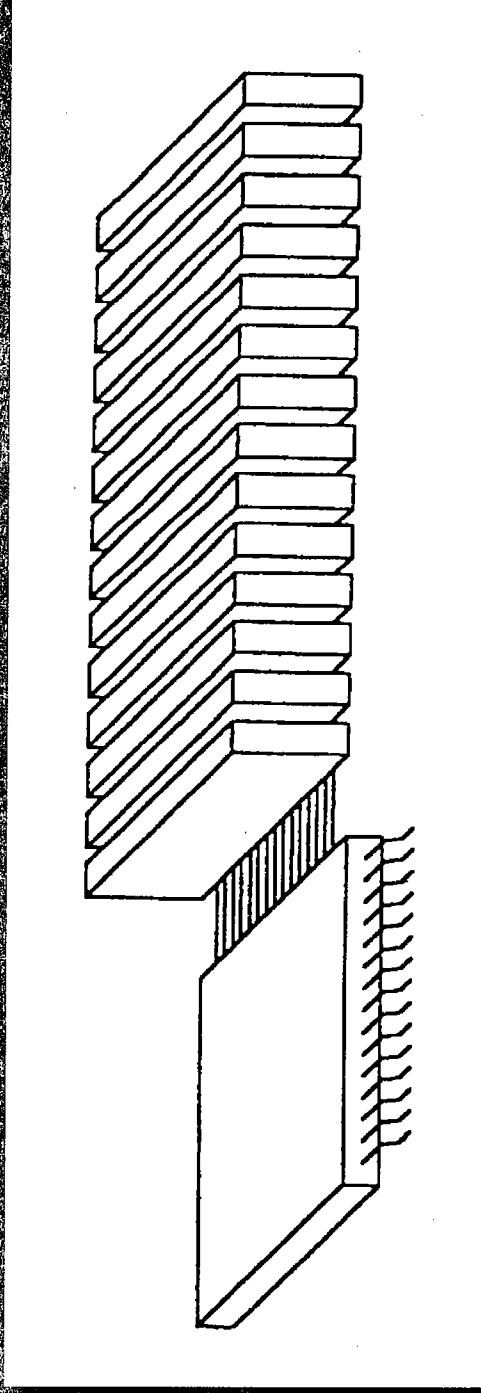


Illustration based on CX1543 at 7

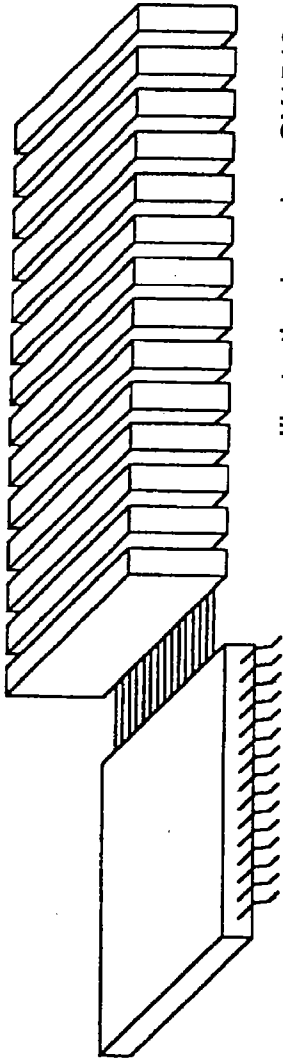
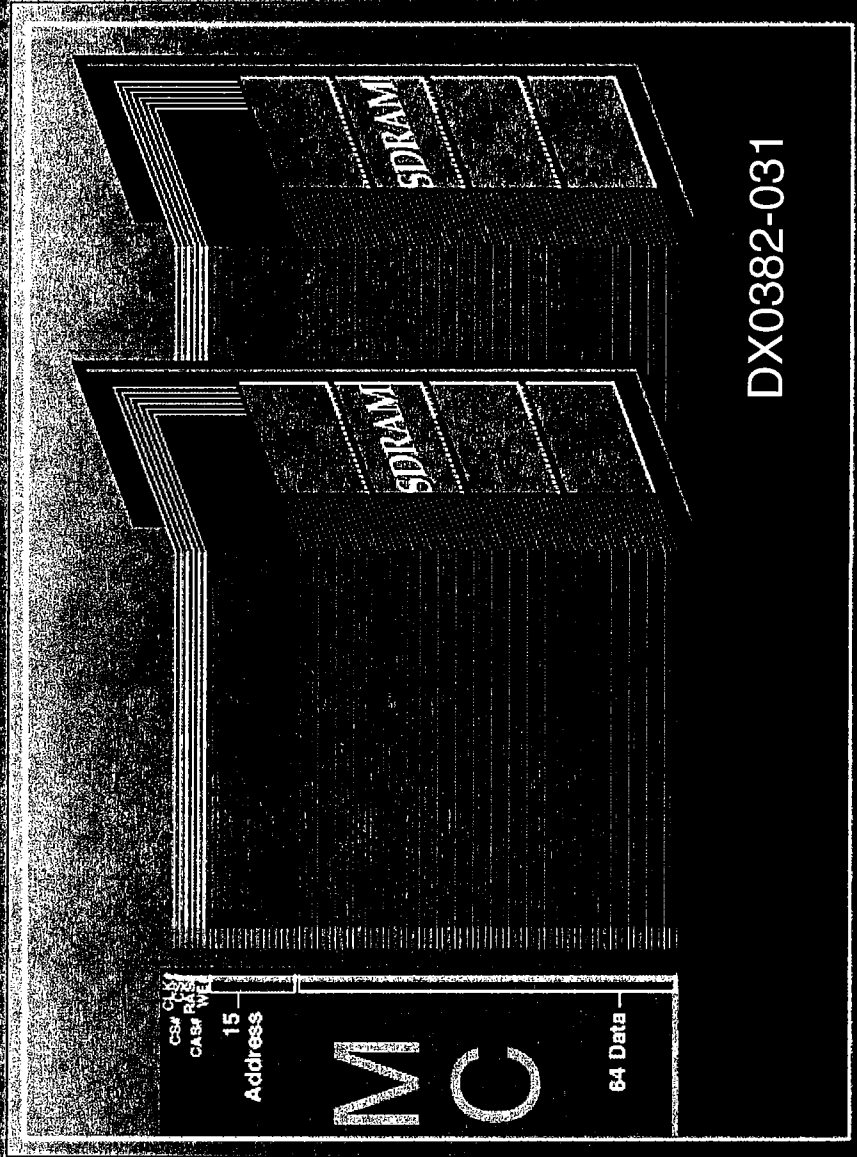


Illustration based on CX1543 at 7



DX0382-031