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To: Norbert Holtkamp

From: Tom Shea

Subject: **Sixth report of the LLRF Advisory Board**

Introduction

The following LLRF Advisory Board (LAB) members contributed to this report:
Tom Shea (ORNL, Chairman)
Curt Hovater (JLab)
Mike Thuot (LANL)
Coles Sibley (ORNL).

Assessment

Planning and budget: Burn rates at each lab have been assessed and the team leaders have determined that LLRF will stay within budget for FY03. After initial testing of the new hardware platform, production costs can be estimated to assess budget risk for FY04.

Initial System: Conditioning of DTL Tank 3 has been performed under the control of the initial LLRF system. One lesson learned from this experience and from Front End operation is the importance of automatic startup. This is an ongoing priority for the software team. Data from cryomodule tests at Jlab have been analyzed and some tests must be repeated. There appears to be time in the schedule for these additional tests. Hardware for the remaining DTL Tanks is arriving in time for integration and commissioning.

Ultimate system: Initial integration of the new (Rev 0) hardware is in progress. Although closed loop operation has not yet been demonstrated, the team has achieved significant success. After initial testing in the PCI environment, the new Digital Front End (DFE), Analog Front End (AFE), and RF output (RFO) modules were integrated into the final VXI environment. Data flow through all hardware and software components was demonstrated. It appears that only minor revisions will be necessary on each circuit. This demonstrates that the thorough engineering and review of these designs has paid off. A few weeks of schedule slip has occurred, but schedule and technical risk in this area remains manageable.

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Software and Gate Array Development: Complete specifications and test plans for the gate array code and IOC software have not been produced. This has made it difficult to add resources and assess progress. Work on the new gate array code currently consists of translating firmware to VHDL and then porting it from the initial to the ultimate system. This appears to be going well. The scalability of the original architecture has not yet been demonstrated, so rewrites might be needed on the way to the SCL systems. Over the past several months, the LLRF hardware and software engineers have met frequently and formed a strong and effective team. The successes noted above are evidence of this. In the end, this is more important than the development of a formal specification. However, until most functionality required for the SCL is demonstrated on the ultimate system, schedule risk remains high.

Recommendations

Develop a cost estimate for the production hardware.

Identify critical functionality to be provided by the gate array code and IOC software. Use this to redefine the milestones for the team.