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Date: February 7, 2003

To: Norbert Holtkamp

From: Tom Shea

Subject: **Fourth report of the LLRF Advisory Board**

Introduction

The following LLRF Advisory Board (LAB) members contributed to this report:
Tom Shea (ORNL, Chairman)
Curt Hovater (JLab)
Craig Swanson (ORNL/AlphaCad)
Mike Thuot (LANL)
Coles Sibley (ORNL)

At this time, Craig Swanson leaves the Advisory Board to work full time for the LLRF team. We have appreciated his expert assessment of gate array issues and know that he will provide valuable contributions in his new role. In the future, Coles Sibley will cover these issues for the board.

Assessment

The LLRF team continues to make good progress. As described below, they have responded to the three recommendations contained in our last report:
Integration of the resource-loaded plans: Resource loaded schedules have been used to back up the team's budget request. Team leaders from all three labs agree that the proposed work is adequately funded. This concurrence is required to assure success. Next week, we expect to see the complete documentation for the Project Change Request and will then comment on the remaining risk.
Completion of the specification and ICD for the ultimate system
The phase error budget has been significantly refined and is now integrated with the reference line design. This good work should continue. The ICD remains to be completed.
Preparation of a detailed response to the FCM review.
The team released this document last week. Overall, we believe that the committee's concerns are being adequately addressed. We will continue to track their progress in closing out each item.

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We have also observed significant progress in the following areas:
Initial System. Operation of the initial system was demonstrated near the end of Front End commissioning at Oak Ridge. The lessons learned during this experience should be documented in time to affect development of the ultimate system. Preparations for the JLab test continue on schedule, although the date of this test has been delayed slightly for reasons unrelated to LLRF. We are encouraged to see that resources from all labs will support this test.
Hardware Development. Hardware development remains on schedule with completion of the DFE schematic. The CAD group at LANL has demonstrated that the board is routable. This can be challenging with dense BGA packaging. Problems were avoided by keeping design simple. Schedule risk in this area is currently low, but this will be reevaluated when the prototype hardware is tested.

Currently, we believe that schedule risk is dominated by **Software and Gate Array Development Activities**. This risk can be managed by producing a detailed specification for the gate array code and the IOC software. To assure consistency, the initial specification should be approved by a single system architect. We assume that this person is Larry Doolittle, who has recently been acting in this role. We know that the team is already hard at work on this specification. Given this documentation, we believe that the team has the experience to successfully manage this complex development project.

Recommendations

Release a functional specification for the software and gate array code

Document lessons learned during operation of the initial system.

The next LAB report will be released February 28, 2003